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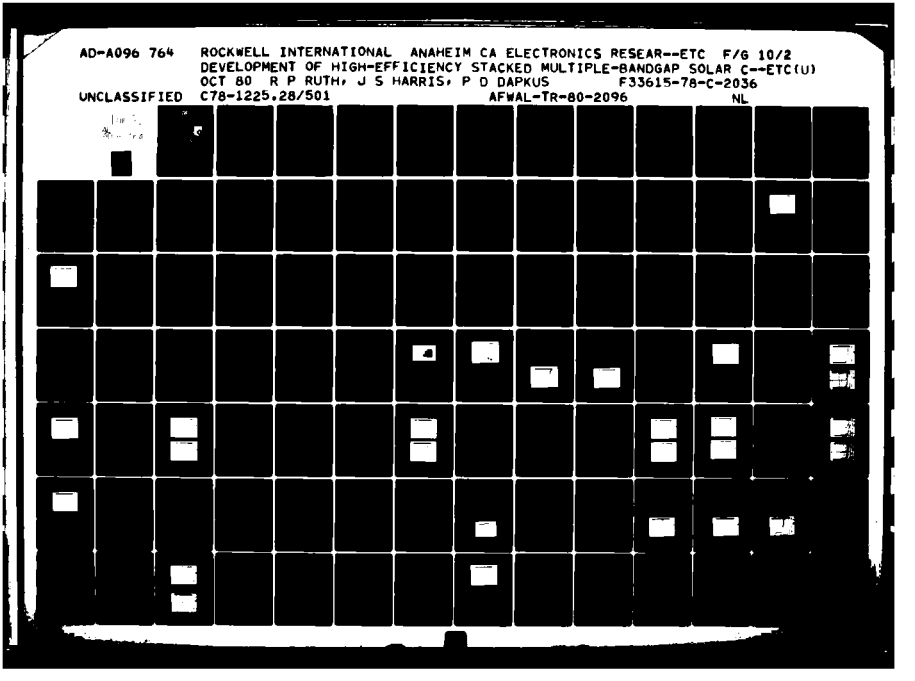

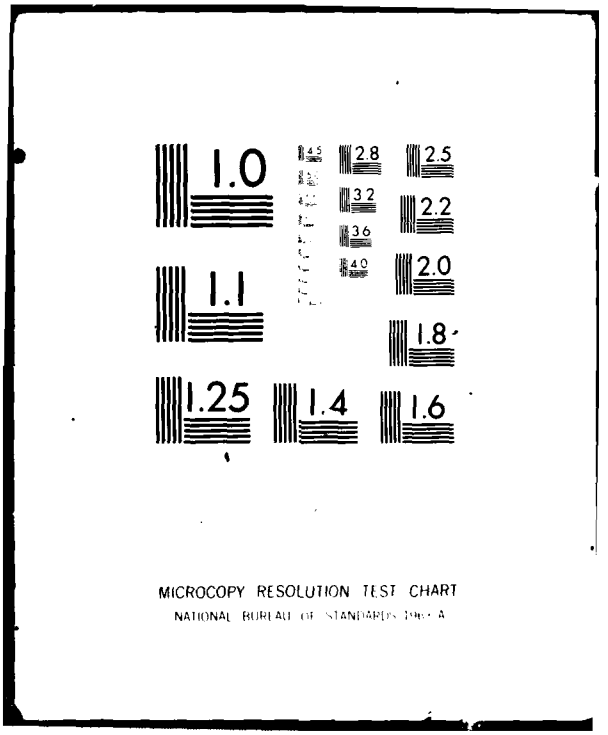
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DEVELOPMENT OF HIGH-EFFICIENCY STACKED MULTIPLE-BANDGAP SOLAR CELLS

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This technical report has been reviewed and is approved for publication.

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The first 14-month program of a twenty-four month experimental investigation backed by analytical modeling has been conducted to develop technologies required for fabricating stacked multiple bandgap solar cell (SMBSC) assemblies having AM0 1-sun efficiencies of 25% or greater at 25°C.

Investigations were undertaken with the following four SMBSC materials systems: (1) two-cell GaAs-Ge structure, made by metalorganic chemical vapor deposition (MO-CVD), conventional CVD, and molecular-beam epitaxy (MBE) methods; (2) two-cell GaAs-InGaAs structure, made by liquid-phase epitaxy (LPE) techniques; (3) three-cell

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GaAlAs-GaAs-GaAsSb structure, made by MO-CVD and MBE methods; and (4) three-cell GaAlAs-GaAs-InGaAsP structure, made by LPE and MBE methods. Each of these systems involves the GaAlAs-GaAs materials combination as the basic building block. Near the end of the program a change in emphasis was introduced to limit the investigations to GaAlAs-GaAs and GaAs-Ge two-cell structures and the three-cell GaAlAs-GaAs-Ge structure that might also result. Principal emphasis was then placed on the MO-CVD technique, supplemented by MBE, LPE, or other deposition and/or processing techniques where appropriate.

The principal achievement was with the GaAlAs-GaAs system, in which a two-cell SMBSC that exhibited voltage addition ($V_{oc} \geq 2.1$ V) under illumination was successfully fabricated. The two individual cells and the connecting tunnel junction were grown entirely by MO-CVD techniques in this structure. Similar structures made by a combination of MO-CVD and MBE techniques also appeared quite promising.

Two-cell GaAs-Ge assemblies, made by a combination of MO-CVD and conventional CVD methods or by combined MO-CVD and MBE techniques, were not as successful, although theoretically capable of essentially the same overall efficiency (up to ~25%) as the GaAlAs-GaAs tandem structure. The other materials combinations investigated in this program received considerably less attention, and correspondingly less progress toward the program goals was made with those structures.

Details of the investigations with all four materials systems are given, and recommendations for continued work are outlined.

FOREWORD

This report was prepared by Rockwell International Electronics Research Center Laboratories in Anaheim and Thousand Oaks, California, under contract F33615-78-C-2036.

The work was administered under the direction of W. P. Rahilly, AFWAL/P00C-2, Air Force Wright Aeronautical Laboratories, Aero Propulsion Laboratory, under Project 3145, Task 314519, Development of High-Efficiency Stacked Multiple-Bandgap Solar Cells. The period covered is 1 August 1978 to 1 October 1979. Contributors include L. A. Moudy, K. L. Hess, F. F. Kinoshita, R. E. Johnson and R. D. Yingling of the Electronics Research Center, Anaheim laboratories, and Y. Z. Liu and R. Sahai of the Electronics Research Center, Thousand Oaks laboratories.

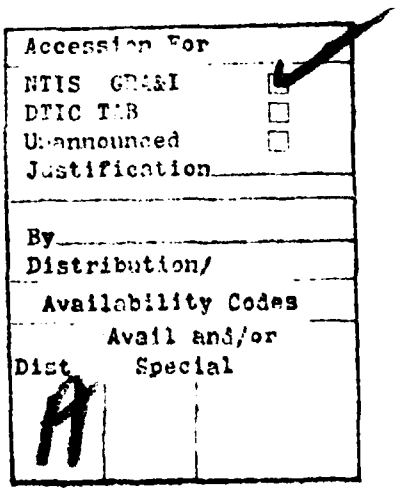


TABLE OF CONTENTS

Section			Page
1	INTRODUCTION AND SUMMARY OF RESULTS		1
	1.1	Technical Concepts	1
	1.2	Program Objectives	5
	1.3	General Technical Approach and Program Rationale	6
	1.4	Summary of Principal Results	7
2	DETAILED DISCUSSION OF RESULTS		17
	2.1	SMBSC Modeling and Analysis	18
		2.1.1 Multilayer AR Coating Design	19
		2.1.2 Ge Solar Cells	20
		2.1.3 GaAlAs Heteroface Solar Cells	24
		2.1.4 GaAs Window-type Solar Cells	25
	2.2	GaAs-Ge SMBSC Technology Development	28
		2.2.1 Properties of GaAs-Ge Interface	30
		2.2.2 GaAs Solar Cells for GaAs-Ge SMBSC's	30
		2.2.3 Ge Solar Cells for GaAs-Ge SMBSC's	63
		2.2.4 Connecting Intercell Junction Structures for GaAs-Ge SMBSC's	84
		2.2.5 Experimental GaAs-Ge SMBSC Structures	94
	2.3	GaAs-InGaAs SMBSC Technology Development	98
		2.3.1 InP and InGaAs Layers Grown by LPE	99
		2.3.2 AlGaAsSb Materials System as Alternative for Low-bandgap Cell	106
	2.4	GaAlAs-GaAs-GaAsSb SMBSC Technology Development	113
		2.4.1 GaAlAs Solar Cells	115
		2.4.2 Connecting Junctions in GaAs and GaAlAs	129
		2.4.3 GaAlAs-GaAs Two-cell SMBSC's	132
	2.5	GaAlAs-GaAs-InGaAsP SMBSC Technology Development	142
		2.5.1 LPE Growth of GaAlAs on GaAs Substrates	143
		2.5.2 LPE Growth of InGaAsP	149
	2.6	Development of AR Coating Technology	150
3	SUMMARY AND CONCLUSIONS		151
4	REFERENCES		162

LIST OF ILLUSTRATIONS

Figure		Page
1.	Schematic Representation of Stacked Multiple-bandgap Solar Cell	3
2.	Schematic Representation of SMBSC Configuration Involving Both Electrical and Optical Series Arrangement	4
3.	Tunneling I-V Characteristic for 25x25 mil Mesa Diode in p^+GaAs:Zn/n^+GaAs:Se Epitaxial Structure Grown by MO-CVD on nGaAs:Si Substrate at 650°C	10
4.	Configuration of Two-cell GaAlAs-GaAs SMBSC for which Voltage Addition was Observed under Illumination	11
5.	Dark and Illuminated (microscope lamp) I-V Curves for Two-cell SMBSC Grown Entirely by MO-CVD on GaAs:Si Substrate, with $Ga_{0.7}Al_{0.3}As$ Cell and GaAs Cell Connected by Intermediate n^+-p^+ Junction in GaAs	12
6.	Optimized 3-layer AR Coating Design for AM0 Spectrum with 4062Å CaF_2 Top Layer, 838Å SiO_2 Middle Layer, and 591Å TiO_2 Bottom Layer for 0.3-1.1μm Operation (3-cell SMBSC) and Minimum Integrated Reflection Loss	21
7.	Optimized 3-layer AR Coating Design for AM0 Spectrum with 1810Å MgF_2 Top Layer, 919Å SiO_2 Middle Layer, and 1296Å TiO_2 Bottom Layer, for 0.3-1.8μm Operation (2-cell or 4-cell SMBSC) and Minimum Integrated Reflection Loss	21
8.	Optimized 3-Layer AR Coating Design for AM0 Spectrum with 1756Å MgF_2 Top Layer, 1340Å SiO_2 Middle Layer, and 835Å Ta_2O_5 Bottom Layer, for 0.3-1.8μm Operation (2-cell or 4-cell SMBSC) and Maximum Short-circuit Current for Cell Assembly	22
9.	Calculated Internal Photoresponse (charge collection efficiency) for Ge Solar Cell of Specified Parameters	22
10.	Calculated Internal Photoresponse (charge collection efficiency) for Thin Ge Solar Cell with and without Back-surface Field Associated with n-n^+ Junction at Back of Cell	24
11.	Measured and Calculated Photoresponse Data for As-grown GaAlAs Solar Cell of Sample LPE1011, Based on Corrected Experimental Photoresponse Curve and Computer Model Using Parameters of Table 3	26
12.	Two Possible Configurations of GaAs-Ge Two-cell SMBSC Assembly	29
13.	Photograph of Typical Array of 0.5 cm x 0.5 cm GaAlAs-GaAs Cells Grown by MO-CVD and Fabricated on Single-crystal GaAs Substrate ~3.7 cm x 2.1 cm	32
14.	Illuminated (microscope lamp) I-V Characteristics of Conventional GaAlAs-GaAs Thin-window Heteroface Solar Cell Structure Grown by MO-CVD at 750°C on GaAs Single-crystal Substrate, Showing Effect on Fill Factor of Centering Illumination (a) Near Metal Contact Pad at Edge of 0.5cm x 0.5cm Cell, and (b) Near Opposite Edge of Cell	33

LIST OF ILLUSTRATIONS (Cont)

Figure		Page
15.	Dark and Illuminated (microscope lamp source) I-V Characteristics of GaAℓAs-GaAs Window-type Solar Cell Grown by MO-CVD on Single-crystal GaAs:Si Substrate Early in Phase 1 Program ...	34
16.	Dark and Illuminated (microscope lamp) I-V Characteristics of 0.5cm x 0.5cm GaAℓAs-GaAs Window-type Solar Cell Deposited by MO-CVD at~ 750°C on (100) GaAs:Si Substrate Midway through Phase 1 Program	35
17.	Dark and Illuminated (microscope lamp) I-V Characteristics of GaAℓAs-GaAs Thin-window Heteroface Solar Cell Grown by MO-CVD at 750°C on (100) GaAs:Si Substrate	37
18.	Dark and Illuminated (xenon lamp AM0 simulator, 135 mw/cm^2) I-V Characteristics of GaAℓAs-GaAs Thin-window Heteroface Solar Cell grown by MO-CVD at 750°C on Same (100) GaAs:Si Substrate as Cell of Figure 17	37
19.	Dark and Illuminated (microscope lamp) I-V Characteristics of Conventional Thin-window GaAℓAs-GaAs Heteroface Cell (0.5cm x 0.5cm) Grown by MO-CVD at ~700°C on Single-crystal GaAs:Te Substrate	39
20.	Dark and Illuminated (microscope lamp) I-V Characteristics of Conventional Thin-window GaAℓAs-GaAs Heteroface Cell (0.5 cm x 0.5 cm) Grown by MO-CVD at ~750°C on Single-crystal GaAs:Te Substrate	39
21.	Dark and Illuminated (microscope lamp) I-V Characteristics of Thin-window GaAℓAs-GaAs Heteroface Solar Cell (0.5cm x 0.5cm) Grown by MO-CVD at ~750°C on Single-crystal GaAs:Te Substrate; Both Window Layer and p-type Active Layer Thinner than Usual	40
22.	Fourth-quadrant I-V Characteristic of GaAℓAs-GaAs Window-type Heteroface Solar Cell (0.5cm x 0.5cm) Made by MO-CVD, under Simulated AM0 Illumination of 129 mw/cm^2 from Calibrated Simulator	40
23.	Dark and Illuminated (microscope lamp) I-V Curves of Two Conventional GaAℓAs-GaAs Thin-window Heteroface Solar Cells (0.5cm x 0.5cm) Grown by MO-CVD at 750°C on Different Single-crystal GaAs Substrates after Recalibration of Mass Flow Controller.....	42
24.	Spectral Response Data for Two Different GaAℓAs-GaAs Heteroface Solar Cells (0.5cm x 0.5cm) Processed in MO-CVD Layers Grown at 750°C on One GaAs Substrate Wafer.....	43
25.	Dark and Illuminated I-V Characteristics of GaAs p-n Junction Mesa Diodes (50 mil x 50 mil) Grown by MO-CVD on n-type (100)Ge Substrates; a) Uncoated Substrate; b) Substrate Coated with SiO_2	46
26.	Dark and Illuminated I-V Characteristics of GaAℓAs-GaAs Solar Cells Grown by MO-CVD at 700°C Simultaneously on a) Single-crystal (100)GaAs:Si Substrate and b) Single-crystal (100)Ge:Sb Substrate with SiO_2 Coating	47

LIST OF ILLUSTRATIONS (Cont)

Figure		Page
27.	Forward Dark I-V Characteristics of GaAlAs-GaAs Solar Cells Grown by MO-CVD on GaAs:Si Substrates and Processed into Completed Devices a) in Sixth Month of Program and b) Early in Program	48
28.	Dark and Illuminated (microscope lamp) I-V Characteristics of GaAlAs-GaAs Heteroface Solar Cells (0.25 cm^2 area) Grown by MO-CVD at ~690°C on a) (100) Ge:Sb Single-crystal Substrate and b) (100) GaAs:Si Single-crystal Substrate	50
29.	Dark and Illuminated (microscope lamp) I-V Characteristics of GaAlAs-GaAs Heteroface Solar Cells (0.25 cm^2 area) Grown by MO-CVD at ~700°C on a) (100) Ge:Sb Single-crystal Substrate and b) (100) GaAs:Si Single-crystal Substrate, with Different Predeposition Conditions in Reactor Chamber from Those Used for Cells of Figure 28	51
30.	Dark and Illuminated (microscope lamp) I-V Characteristics of GaAlAs-GaAs Thin-window Heteroface Solar Cell (0.5cm x 0.5cm) Grown by MO-CVD at 750°C Using "Non-standard" Predeposition Procedure on a) Ge:Sb Substrate and b) GaAs:Si Substrate	53
31.	Dark and Illuminated (microscope lamp) I-V Characteristics of GaAlAs-GaAs Thin-window Heteroface Solar Cell (0.5cm x 0.5cm) Grown by MO-CVD at 750°C on Ge:Sb Substrate Using Standard Predeposition Procedure	54
32.	Dark and Illuminated (AM0 simulator, ~135 mw/cm^2) I-V Characteristics of Another GaAlAs-GaAs Thin-window Heteroface Solar Cell (0.5cm x 0.5cm) Fabricated on Same Ge:Sb Substrate as Cell of Figure 31	54
33.	Fourth Quadrant of Illuminated (AM0 simulator) I-V Curve for MO-CVD GaAs Heteroface Solar Cell (0.5cm x 0.5cm) Grown at ~750°C on (100)Ge:Sb Substrate, Using Standard Pre-AsH_3 Procedure	56
34.	Fourth Quadrant of Illuminated (AM0 simulator) I-V Curve for MO-CVD GaAs Heteroface Solar Cell (0.5cm x 0.5cm) Grown at ~750°C on (100)Ge:Sb Substrate Using Nonstandard Pre-AsH_3 Procedure	57
35.	Spectral Response Curves for GaAs Heteroface Cells Made by MO-CVD on GaAs and Ge Substrates; Junction Depths Nominally Equal in Both Cells	59
36.	Illuminated (AM0 simulator) I-V Curve for GaAs Heteroface Solar Cell (area 0.025 cm^2) Grown by MBE at ~580°C on (100) GaAs Substrate	60
37.	Illuminated I-V Curves for GaAs n/p Solar Cell Structure (area 0.025 cm^2) Grown by MBE on n-type (100) Ge Substrate, for Several Different Levels of Illumination from Microscope Lamp.	61
38.	Spectral Response Curve for MBE-grown Device of Figure 37, Showing Photoresponse of Opposite Sense for n/p GaAs Junction and pGaAs-nGe Heterojunction	62

LIST OF ILLUSTRATIONS (Cont)

Figure		Page
39.	Dark and Illuminated (microscope lamp source) I-V Characteristics of Ge p-n Junction Mesa Diode Grown by MO-CVD on Single-crystal Ge:Sb Substrate	64
40.	Dark and Light (microscope lamp source) I-V Characteristics of Ge p-n Junction Solar Cell Grown by GeH_4 Pyrolysis on Single-crystal (100)Ge:Sb Substrate	65
41.	Dark and Light (microscope lamp source) I-V Characteristics of Ge p-n Junction Mesa Diode Grown by GeH_4 Pyrolysis on Single-crystal (100)Ge:Sb Substrate	66
42.	Resistivity as Function of Depth into Sample as Obtained by Spreading Resistance Probe Scan on Beveled Surface in Two-layer CVD Ge Film Grown at 650°C on n-type GaAs Surface; p-n Junction Shown Is at Interface between p-type and n-type Ge Layers	68
43.	Dark and Illuminated (microscope lamp) I-V Curves for Ge p-n Junction Mesa-type Solar Cell Grown by CVD at ~680°C on GaAs:Te Substrate	70
44.	Dark and Illuminated (microscope lamp) I-V Curves for Ge p-n Junction Solar Cell (0.5 cm x 0.5 cm) Grown by CVD at ~680°C on Ge:Sb Substrate	70
45.	Spreading Resistance Data for Undoped Ge Films Grown by CVD on Single-crystal Substrates of n-type (100)Ge:Sb in Two Separate Deposition Experiments, Showing Effects of Possible Ga Doping of Ge Films; a) Deposition Temperature 750°C, Deposition Time 60 min; b) Deposition Temperature ~760°C, Deposition Time 230 min	72
46.	Spreading Resistance Data (as function of depth) for B-doped p-type Ge Film Grown by CVD at 800°C on Substrate of Single-crystal n-type (0.02-0.03 ohm-cm) Ge:Sb	73
47.	Dark and Illuminated (microscope lamp) I-V Curves for Ge p-n Junction Solar Cell (0.5 cm x 0.5 cm) Formed by p-type B-doped Ge Deposition (CVD) on n-type Ge:Sb (0.03 ohm-cm) Substrate at 800°C at Rate of ~1900 Å/min	75
48.	Fourth Quadrant of Illuminated (AM0 simulator) I-V Curve for Ge CVD Cell No. 75-7, Grown at ~800°C on (100)-oriented n-type 0.03 ohm-cm Ge Substrate Wafer	78
49.	Dark Forward I-V Curve for Ge CVD Cell No. 75-7	79
50.	Relative Spectral Photoresponse of CVD Ge Solar Cells No. 75-7 and No. 73-11	80
51.	Fourth Quadrant of Illuminated (AM0 simulator) I-V Curves for CVD Ge Solar Cell No. 79-9 before and after Contact Alloying Procedure	81
52.	Dark and Illuminated (AM0 simulator) I-V Curves Obtained for CVD Ge Cell No. 73-11 after Contact Alloying Procedure, Showing Gradual Shift in Illuminated Curve over Period of ~15 sec following Exposure to Light	81

LIST OF ILLUSTRATIONS (Cont)

Figure		Page
53.	Dark and Illuminated (microscope lamp) I-V Curves for Solar Cell (area 6.6 x 10^{-3} cm^2) Formed by Diffusing MBE-deposited As into p-type (100)Ge Substrate, Showing Effect of Variation of Incident Intensity	83
54.	Relative Spectral Photoresponse for n/p Ge Solar Cell Made by MBE Deposition of As onto p-type (100)-oriented Ge Substrate Wafer Followed by Thermal Diffusion of the As	83
55.	Spreading Resistance Data for n-type Ge Single-crystal Wafer with p-n Junction 2.0μm Deep Formed by Diffusion of Ga at 850°C for 5 hr in He, Using Spin-on Oxide Diffusion Source	85
56.	Tunneling I-V Characteristic for 25x25 mil Mesa Diode in p^+GaAs:Zn/n^+GaAs:Se Epitaxial Structure Grown by MO-CVD on nGaAs:Si Substrate at 650°C	86
57.	I-V Characteristic of GaAs:Se/GaAs:Zn n^+/p^+ Tunnel Junction Structure Grown by MO-CVD at ~650°C on GaAs Single-crystal Substrate	87
58.	I-V Characteristic of GaAs:Se/GaAs:Zn n^+/p^+ Tunnel Junction Structure Grown by MO-CVD at ~630°C on GaAs Single-crystal Substrate	88
59.	I-V Characteristic of n^+/p^+ GaAs:Se/GaAs:Be Hybrid Tunnel Structure Made by Growing MO-CVD Layer on Previously Grown MBE Layer on Single-crystal GaAs Substrate	89
60.	Dark Log I-V Curve for Hybrid MO-CVD/MBE n^+GaAs/p^+GaAs Tunnel Junction Structure on GaAs Substrate	89
61.	Dark Log I-V Curve for n^+GaAs/p^+GaAs Tunnel Junction Structure Grown Entirely by MO-CVD on GaAs Substrate	90
62.	I-V Characteristic of p^+/n^+ GaAs:Zn/GaAs:Se Tunnel Diode Structure Grown by MO-CVD at ~630°C on Single-crystal GaAs Substrate	91
63.	Configuration of n^+/p^{++} Conducting Junction Structure Formed by MBE on Single-crystal GaAs Substrate at ~540°C	92
64.	Typical Forward and Reverse Oscilloscope Trace Obtained with n^+/p^{++} GaAs Conducting Junction Structure Grown by MBE at ~540°C on p^+GaAs:Zn Substrate, Showing Ohmic Behavior	92
65.	Forward and Reverse I-V Characteristics of n^+/p^{++} GaAs Conducting Junction Structure of Figure 64 Grown by MBE at ~540°C on p^+GaAs:Zn Substrate, after Temperature Cycling Duplicating that Encountered in LPE Cell Growth	94
66.	Forward and Reverse I-V Characteristics of $n/n^+/p^+/p$ GaAs Conducting Junction Structure Grown by MBE on p^+GaAs:Zn Substrate (a) before and (b) after Temperature Cycling Duplicating that Encountered in LPE Cell Growth	95
67.	Probable Configuration of GaAs-Ge Two-cell SMBSC Made Entirely by CVD Techniques	96

LIST OF ILLUSTRATIONS (Cont)

Figure		Page
68.	Spectral Response Curve for MBE-grown Stacked Two-cell Structure Having Apparent Configuration $p^+Ga_{0.2}Al_{0.8}As/nGaAs/n^+GaAs/p^+GaAs/nGe$	97
69.	Spectral Photoresponse of LPE InGaAs p-n Junction Cell with Illumination Incident through InP Substrate	101
70.	Dark and Illuminated I-V Characteristics of InGaAs p-n Junction Measured with Microscope Lamp Illumination	102
71.	Dark and Illuminated (microscope lamp) I-V Curves Obtained for Different Intensities of Illumination for InP/InGaAs Solar Cell (0.025 cm x 0.025 cm) Obtained by LPE Growth of Undoped n-type InGaAs Layer on Single-crystal p^+InP Substrate Wafer	105
72.	Relative Spectral Response Curve for InP/InGaAs Window-type Solar Cell Grown by LPE	106
73.	Dark and Illuminated (AM1 simulator) I-V Characteristics of pGaSb/nGaSb Solar Cell (area 0.025 cm^2) a) with Al GaAsSb Window Layer and b) without Window Layer	108
74.	Spectral Response of pAlGaAsSb/pGaSb/nGaSb Window-type Solar Cell of Figure 73a.	109
75.	Dark and Illuminated (AM1 simulator) I-V Characteristics of LPE-grown p^+GaAl AsSb/pGaAl Sb/nGaSb Window-type Solar Cells	111
76.	Dark and Illuminated (microscope lamp source) I-V Characteristics of 50 mil x 50 mil Mesa Diode Fabricated in $Ga_{0.63}Al_{0.37}As$ p-n Junction Structure Grown by MO-CVD on (100)GaAs Substrate	116
77.	I-V Characteristic of p-n Junction Mesa Diode in $Ga_{0.6}Al_{0.4}As$ Structure Grown by MO-CVD on GaAs:Si Substrate	116
78.	Dark and Illuminated (microscope lamp) I-V Curves for Thin-window Solar Cell (0.5cm x 0.5cm) in $Ga_{0.6}Al_{0.4}$ As Grown by MO-CVD at 700°C on GaAs:Te Substrate	117
79.	Configuration of $Ga_{0.7}Al_{0.3}As$ Window-type Solar Cell Structure Grown by MO-CVD on GaAs Substrate	118
80.	Dark and Illuminated (microscope lamp) I-V Curves for Window-type $Ga_{0.7}Al_{0.3}As$ p-n Junction Solar Cell (0.5cm x 0.5cm) Grown by MO-CVD at ~790°C on GaAs:Te Substrate	119
81.	Dark and Illuminated (microscope lamp) I-V Curves for 0.5cm x 0.5cm Window-type $Ga_{0.7}Al_{0.3}As$ p-n Junction Solar Cell Grown by MO-CVD at 750°C on GaAs Substrate	120
82.	Spectral Response Data for Two 0.5cm x 0.5cm $Ga_{0.7}Al_{0.3}As$ Alloy Solar Cells Grown by MO-CVD at 750°C on Common GaAs:Si Substrate	121
83.	Dark and Illuminated (microscope lamp) I-V Curves for Window-type $Ga_{0.76}Al_{0.24}As$ p-n Junction Solar Cell (0.5cm x 0.5cm) Grown by MO-CVD at ~750°C on (100)GaAs:Te Substrate	122

LIST OF ILLUSTRATIONS (Cont)

Figure		Page
84.	Illuminated I-V Curve (fourth quadrant) of $Ga_{0.76}Al_{0.24}As$ Solar Cell from Same Array as that of Figure 83 but Obtained with AM0 Simulator	123
85.	Dark and Illuminated (microscope lamp) I-V Curves for Window-type $Ga_{0.7}Al_{0.3}As$ p-n Junction Solar Cell (0.5cm x 0.5cm) Grown by MO-CVD at ~790°C on (100)GaAs:Si Substrate	124
86.	Measured V_{OC} Values for MO-CVD Alloy Cells of Tables 8 and 9 as Function of Deduced Al Content of Junction-forming Layers, for Simulated AM0 Illumination	128
87.	Dependence of J_{SC} upon Junction Depth (p layer thickness) for Three $Ga_{0.8}Al_{0.2}As$ Solar Cells Made by MO-CVD, for Simulated AM0 Illumination	128
88.	Spectral Response Curves for Three MO-CVD $Ga_{0.8}Al_{0.2}As$ Cells of Different Junction Depths (p layer thickness)	130
89.	Spectral Photoresponse Curves for GaAlAs Solar Cells Made in MO-CVD Structures Having Different GaAlAs Window-layer Compositions, Processed Both in As-grown Condition and with Zn Diffusion	130
90.	Configuration of Two-cell SMBSC Grown by MO-CVD on GaAs Single-crystal Substrate, with Connecting Junction in GaAlAs	132
91.	Dark and Illuminated (microscope lamp) I-V Characteristics of Two-cell SMBSC Grown by MO-CVD, with $Ga_{0.6}Al_{0.4}As$ Cell and GaAs Cell Connected by Intermediate n^+-p^+ Junction in $Ga_{0.92}Al_{0.08}As$	133
92.	Dark and Illuminated (microscope lamp) I-V Characteristics of Two-cell SMBSC Grown by MO-CVD, with $Ga_{0.6}Al_{0.4}As$ Cell and GaAs Cell Connected by Intermediate n^+-p^+ Junction in GaAs	134
93.	Dark and Illuminated (microscope lamp) Reverse I-V Characteristics of Two-cell $Ga_{0.6}Al_{0.4}As$-GaAs SMBSC Represented in Figure 92	134
94.	Configuration of Two-cell GaAlAs-GaAs SMBSC for which Voltage Addition was Observed under Illumination	135
95.	Dark and Illuminated (microscope lamp) I-V Curves for Two-cell SMBSC Grown Entirely by MO-CVD on GaAs:Si Substrate, with $Ga_{0.7}Al_{0.3}As$ Cell and GaAs Cell Connected by Intermediate n^+-p^+ Junction in GaAs	136
96.	Modified Configuration of Two-cell GaAlAs-GaAs SMBSC Structure Grown by MO-CVD	137
97.	Dark and Illuminated (microscope lamp) I-V Curves for Two-cell SMBSC Grown Entirely by MO-CVD on GaAs:Si Substrate, with $Ga_{0.7}Al_{0.3}As$ Cell on Top and GaAs Cell on Bottom Connected by Conducting n^+-p^+ Junction in GaAs Intermediate Layer	137

LIST OF ILLUSTRATIONS (Cont)

Figure		Page
98.	Dark and Illuminated (microscope lamp) I-V Curves for Two-cell SMBSC (0.5cm x 0.5cm) Grown by MO-CVD on GaAs:Si Substrate, with $Ga_{0.7}Al_{0.3}As$ Cell on Top (grown at ~775°C) and GaAs Cell on Bottom, Connected by n^+/p^+ Conducting Junction in GaAs Intermediate Layer Grown at ~710°C	138
99.	Configuration of Two-cell GaAlAs-GaAs SMBSC Used to Produce Photoresponse of Figure 100	139
100.	Dark and Illuminated (microscope lamp) I-V Curves for Two-cell SMBSC Grown by MO-CVD on GaAs:Si Substrate, with $Ga_{0.7}Al_{0.3}As$ Alloy Cell on Top and GaAs Cell on Bottom Connected by Conducting n^+/p^+ Junction in GaAs Intermediate Layer	139
101.	Modified Two-cell GaAlAs-GaAs SMBSC Configuration Designed to Give Improved Performance	140
102.	Fourth Quadrant Illuminated (AM0 simulator) I-V Curve for Two-cell SMBSC Made by MO-CVD, Consisting of GaAlAs Cell on GaAs Tunnel Junction on GaAs Cell, All on (100)-oriented GaAs:Si Substrate	141
103.	Three GaAlAs Large-bandgap Solar Cell Structures Grown by LPE Techniques, for Eventual Use in Two-cell and Three-cell SMBSC's	145
104.	Typical a) Illuminated I-V Characteristic and b) Dark Log I-V Characteristic of Zn-diffused-junction Window-type $Ga_{0.61}Al_{0.39}As$ Solar Cell Grown by LPE (Type b, Figure 103)	146
105.	Typical Spectral Photoresponse of Zn-diffused-junction Window-type $Ga_{0.61}Al_{0.39}As$ Solar Cell Grown by LPE (Type b, Figure 103)	147
106	Typical 77°K Photoluminescence Data for Conventional LPE-grown Window-type $Ga_{0.61}Al_{0.39}As$ Solar Cell (Type a, Figure 103)	147
107	Spectral Response Curves for Zn-diffused Heteroface Cell LPE1009 and As-grown Heteroface Cell of Sample LPE1011	149

LIST OF TABLES

Table		Page
1.	Calculated Ideal and Expected AM0 Efficiencies for SMBSC Combinations with Two, Three, or Four Cells	5
2.	Combinations of Materials and Film-growth Techniques Selected for Initial Development in Phase 1 of Program.	7
3.	Parameters Used in Modeling Spectral Photoresponse of LPE-grown Solar Cell (Sample LPE1011)	26
4.	Principal Deposition Parameters, Materials Properties, and AM0 (no AR coating) Photovoltaic Performance Parameters of CVD Ge p/n Solar Cell Structures Grown on Ge Substrates	77
5.	Structural Parameters and Electrical Properties of GaAs Nonrectifying Junction Structures Grown by MBE, before and after Temperature Cycling	93
6.	Material, Fabrication, and Typical Individual Cell Photovoltaic Performance Parameters for Window-type Solar Cell Structures Grown by LPE on n-type GaSb Single-crystal Substrates	110
7.	Summary of Materials and Fabrication Parameters Used in Investigation of Various Ohmic Contacts to p-type and n-type GaSb	112
8.	Principal Physical Parameters of GaAlAs Heteroface Solar Cell Structures Grown by MO-CVD and Processed in Final Two Months of Phase 1	126
9.	Measured Photovoltaic Properties of MO-CVD GaAlAs Heteroface Solar Cells Listed in Table 8 (AM0 simulated illumination)	127
10.	Principal Physical Parameters of LPE GaAlAs Heteroface Solar Cell Structures	145
11.	Measured Photovoltaic Properties of LPE-grown GaAlAs Heteroface Solar Cells Listed in Table 10 (AM0 simulated illumination)	148

1. INTRODUCTION AND SUMMARY OF RESULTS

In recent years, technology developments for the fabrication of high-efficiency solar cells have led to the demonstration of laboratory-type Si and GaAs cells having air-mass-zero (AM0) power conversion efficiencies greater than 15 and 17 percent, respectively. Achievement of significantly higher efficiencies for operation with the space solar spectrum is becoming increasingly important to the Air Force as space power supply performance requirements are increased and the need for weight and cost reductions becomes more evident.

The highest achievable AM0 efficiency for Si solar cells is expected to be in the 16-19 percent range, and the highest efficiency for GaAs cells is expected to be approximately 20-22 percent. Thus, the achievement of solar cell conversion efficiencies greater than 25 percent will require a combination of semiconductor materials processed in some manner such that the resulting devices will have a broader response to the space solar spectrum than that of any of the simple (single-junction) cells. It is anticipated that such a device, in its simplest form, will be monolithic and consist of at least two sub-cell structures of differing bandgap energy connected electrically in series.

The program described in this report is directed toward such a development.

This section of the report describes the basic technical concepts involved, defines the program objectives, outlines the general technical approach employed, and gives a summary of the principal technical results achieved in the first phase (14 months) of the contract.

Section 2 outlines the program plan and schedule followed during the first 14 months of the contract, defines the specific technical tasks that constitute the program, and contains a detailed discussion of the technical activities of Phase 1 and of the results achieved in the period covered by this report.

Section 3 contains a brief discussion of the results and of the conclusions reached therefrom, with recommendations for continued work in Phase 2 of the contract.

Section 4 lists the technical references used throughout the report.

1.1 TECHNICAL CONCEPTS

The GaAs solar cell - whatever specific configuration is involved - is believed to offer the highest ultimate AM0 conversion efficiency of all of the single-component photovoltaic cells developed to the present time, based both on theoretical analyses of the photovoltaic effect at potential barriers in semiconductor materials and on the present state of development of the respective material technologies. However, the prospect of a dramatic increase in cell operating efficiency, even with respect to the present high value of ~19 percent (AM0, 28°C) achieved in the best single-crystal GaAs cells, is offered by the concept of the tandem multiple-bandgap solar cell.

Theoretical analyses by various investigators (Refs 1, 2) have shown that the maximum conversion efficiency for the solar spectrum that can be expected from any one p-n junction type of photovoltaic cell operating at its maximum power point (at ~25°C) is in the 20 to 25 percent range, the specific theoretical maximum depending primarily upon the bandgap energy E_g of the particular semiconductor involved. Analyses of the projected performance of Si and GaAs solar cells under AM0 illumination indicate expected maximum solar conversion efficiencies of about 19 percent for Si and perhaps up to 22 percent for GaAs, with all controllable parameters optimized.

Concentration of sunlight to produce illumination of increased intensity is one method of achieving increased electrical power output per unit area of solar cell surface. However, the approach to more efficient use of the solar spectrum that is addressed in this program is based on the fact that a photovoltaic cell has two major limitations on its ability to convert the incident solar photons, each of energy $h\nu$, into hole-electron pairs that can subsequently be separated, collected, and delivered to an external load. The first is that only those absorbed photons of energy greater than the bandgap energy E_g can produce band-to-band excitation in the semiconductor and thus separation of charges and possible delivery to the load. The second is that all photon energy in excess of the bandgap energy E_g - that is, all of the energy beyond that required to produce a single hole-electron pair - is dissipated internally as heat in the device.

The most efficient response of a p-n junction cell is to photons of energy just exceeding the bandgap energy, so if two or more solar cells of differing bandgap energy (and thus of different composition) could be arranged appropriately to share the solar spectrum, with each operating on that portion of the spectrum to which it is most responsive, a combination converter of overall power efficiency exceeding that of the individual cells used separately in the full solar spectrum could be realized. This concept is not new, having been first proposed by Jackson (Ref 3) in 1955 and examined by various workers at intervals since that time (Refs 4, 5).

There are two principal embodiments of this concept. One involves interposing dichroic mirrors or filters (i.e., beam splitters) in the incident beam of solar radiation so that selected radiation of a portion of the spectrum is diverted to a solar cell whose properties (mainly bandgap energy E_{g1}) allow it to make relatively efficient use of that selected band of radiation, while allowing the remainder of the spectrum to pass on to a second filter/mirror, which again selects a portion of the spectrum to direct onto a second cell of bandgap energy E_{g2}, while transmitting the remainder to a third cell (or a third filter/mirror), and so on.

The other modification of the multiple-cell concept - and the one with potential major impact on space applications - is shown schematically in Figure 1. It can now be seriously considered for practical applications primarily because of the remarkable progress made in thin-film photovoltaic material technologies in the past several years. It involves two or more solar cells of differing composition (and thus differing bandgap energies) used optically in series, in a tandem or stacked arrangement. The cell of largest bandgap energy E_{g1} receives the full solar spectrum incident on its front surface, generating charge pairs from the energy of the absorbed photons of energy greater than E_{g1} and transmitting the radiation of energy $< E_{g1}$ on to the

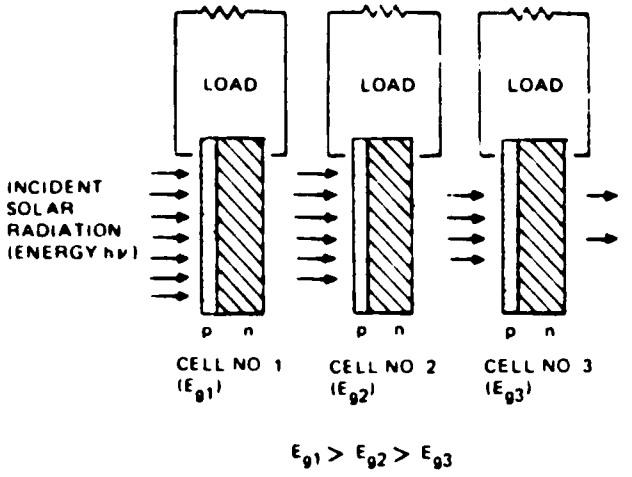


Figure 1. Schematic Representation of Stacked Multiple-bandgap Solar Cell

second cell, of bandgap E_{g2}, which utilizes the narrowed band of energies to generate photovoltage and photocurrent consistent with its photovoltaic properties and transmits the remaining radiation of energy $< E_{g2}$ on to the third cell, if used, and so on.

Although simple in concept, the stacked multiple-bandgap solar cell (SMBSC) involves difficult material problems and design and fabrication complexities. A major problem to be solved is the question of the design of the interface between the back side of the first component and the front side of the cell next in line in the stack. Should the photon-generated current of each cell be extracted separately, as shown in Figure 1, or should the electrical contact be made simply a series connection, with the current leaving the first cell entering the second cell directly – conceptually the simplest structure, and shown in Figure 2? In the latter instance it becomes necessary to match photocurrents of the two adjoining cells at their operating points (not the short-circuit currents), and this requirement alone is accompanied by major difficulties of both material selection and interface design. However, this arrangement is by far the more attractive, since it makes maximum use of the compactness and fabrication advantages of monolithic thin-film semiconductor technologies.

Simplified theoretical models of SMBSC configurations can give rise to a variety of possible cell combinations (more correctly, possible combinations of bandgap energies) that appear to offer very attractive combined conversion efficiencies - some approaching the probable theoretical upper limit of 40 to 50 percent for solar conversion efficiency for a semiconductor-based converter system having no loss of the excess photon energy (Ref 6).

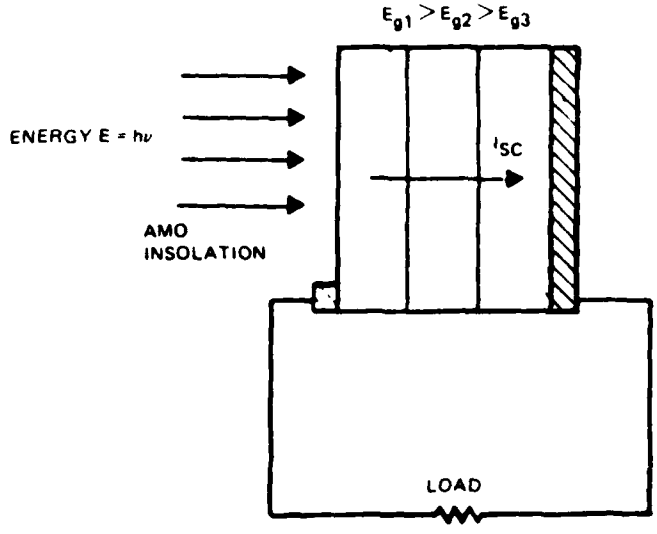


Figure 2. Schematic Representation of SMBSC Configuration Involving Both Electrical and Optical Series Arrangement.

More accurate models of such configurations, however, result in relatively few combinations of either two- or three-cell systems that meet design requirements yet represent material composites that are compatible and fabricatable by presently known technologies. Table 1 shows a summary of the results of preliminary modeling of SMBSC assemblies of the type shown in Figure 2 at Rockwell, using the basic principles that must be applied to the SBMSC concept. Individual cells that compose the two-cell, three-cell, or four-cell stacks are identified by the bandgap energy of the active cell material. The 1.42eV cell involved in each of the combinations listed is the GaAs cell, a point of special significance to be discussed below.

The table gives both theoretical conversion efficiencies for the various combinations, based on idealized junction characteristics and no current collection losses, and realistic projections of efficiencies that could be expected in practical assemblies after adequate development of the particular structures involved, based on empirical data obtained with experimental high-efficiency thin-film GaAs solar cells. The possibility of achieving efficiencies of over 25 percent - possibly greater than 30 percent - is evident from these data, provided the required materials and device technology problems can be adequately solved.

Table 1. Calculated Ideal and Expected AM0 Efficiencies for SMBSC Combinations with Two, Three, or Four Cells

Bandgap Energy	Efficiency (%)							
	Two Cells				Three Cells		Four Cells	
	Ideal η	Expected η	Ideal η	Expected η	Ideal η	Expected η	Ideal η	Expected η
2.0 eV			20.0	14.9	20.0	14.9	20.0	14.9
1.42 eV (GaAs)	26.4	19.8	13.0	9.7	13.0	9.7	13.0	9.7
1.0 eV					7.8	5.6	7.8	5.6
0.8 eV	7.5	4.9					3.5	2.3
Combined η	33.9	24.7	33.0	24.6	40.8	30.2	44.8	32.5

1.2 PROGRAM OBJECTIVES

The overall objective of this program is to develop the necessary technology to fabricate solar cell assemblies having greater than 25 percent power conversion efficiencies at 25°C under space-sunlight illumination of one-sun intensity (AM0, ~135 mw/cm^2).

To achieve this overall objective the following specific technical objectives were defined at the start of the program:

1. Develop and apply rigorous analytical modeling techniques for predicting the performance of SBMSC structures under AM0 operation.

2. Identify and prepare suitable semiconductor, electrical contact, and anti-reflection (AR) coating materials for use in fabricating SMBSC structures involving four (or more) different combinations of semiconductor materials and/or fabrication techniques.

3. Demonstrate and develop an optimized fabrication technology capable of producing large-area (at least 2x2 cm) SMBSC structures exhibiting the specified performance characteristics.

4. Utilize the selected technology for the fabrication of 2x2 cm stacked multiple-bandgap cell assemblies.

5. Test and document the photovoltaic performance and certain radiation damage properties of the fabricated cell assemblies.

The general technical approach used to pursue these objectives is described below.

1.3 GENERAL TECHNICAL APPROACH AND PROGRAM RATIONALE

To pursue the contract objectives and to meet the contractual requirements of 1) investigating four different semiconductor material combinations that can be used for fabricating SMBSC structures and 2) fabricating and delivering 100 solar cell assemblies at the conclusion of the prescribed 24-month experimental performance period (14-month first phase and 10-month second phase), a program involving a combination of analytical modeling and experimental investigations was undertaken.

The program was designed to carry a broad experimental development effort as far as possible before selection of one SMBSC design and fabrication technology for further optimization and subsequent use in preparation of the deliverable cells. The initial development effort necessarily involved fabrication of working device structures in addition to the analytical modeling and the materials investigations. Further, since the technologies involved in SMBSC systems are complex individually and - in most cases - not fully developed in the specific configurations required for the program, significant additional development to integrate the various processes and procedures into a single fabrication technology for preparation of the deliverable assemblies will be required after selection of the identified combination.

The program was based on the following rationale:

1. Semiconductor thin-film technologies that are long-standing specialties of Rockwell ERC - the metalorganic chemical vapor deposition (MO-CVD) process and the liquid-phase epitaxy (LPE) process - are both well-suited to the SMBSC concept.

2. Composite cell modeling and analysis and the experimental development of the identified SMBSC materials combinations should proceed concurrently, with each activity assisting the other.

3. A conservative approach, beginning with two relatively simple two-cell SMBSC combinations involving materials systems with which Rockwell has extensive experience, offers a good chance of early demonstration of a working SMBSC combination at least approaching the program goal of 25 percent overall efficiency.

4. Three-cell (and four-cell) SMBSC combinations to be investigated should be extensions of (and be built upon) the simpler two-cell systems to be investigated and developed first.

Upon consideration of the properties of candidate photovoltaic materials, the available substrate materials, contact materials and interface problems, and the present maturity and anticipated growth of the various material technologies, the GaAlAs/GaAs material system was selected as the basic building block for development of the SMBSC. This material system has been highly developed at Rockwell, with both the MO-CVD technique and the LPE process. The MO-CVD process, in particular, is adaptable to large-scale large-area device production even for structures as complicated as the SMBSC.

The four materials combinations selected for investigation are shown in Table 2. Two of the four materials combinations are two-cell systems and two are three-cell systems that can be expanded to four-cell systems. Table 2 indicates the approximate bandgap energies of the individual cells as well as the film growth technique emphasized in their preparation. All combinations were intended for study at a level of effort such that sufficient information on their device performance as SMBSC's would be obtained by the end of the fourteenth contract month to permit selection of the SMBSC technologies for further development and for fabrication of the deliverable devices at the end of the second phase of the contract.

Table 2. Combinations of Materials and Film-growth Techniques Selected for Initial Development in Phase 1 of Program

SMBSC Type	Approximate Bandgap Energy				Principal Process
	2.0eV*	1.4eV	1.0eV	0.7eV	
1. 2-Cell		GaAlAs/GaAs		Ge	MO-CVD
2. 2-Cell		GaAlAs/GaAs		InP/InGaAs	LPE
3. 3-Cell	GaAlAs	GaAlAs/GaAs	GaAlAsSb/GaAsSb		MO-CVD
4. 3-Cell	GaAlAs	GaAlAs/GaAs	InP/InGaAsP		LPE

*InGaP identified as possible alternate 2.0eV material (both MO-CVD and LPE)

1.4 SUMMARY OF PRINCIPAL RESULTS

The 14-month Phase 1 program involved work in seven main task areas, listed and defined in Section 2 of this report.

Extensive experimental investigation of candidate SMBSC materials systems together with backup analytical modeling led to the successful achievement of a two-cell SMBSC structure in which the two individual cells and the connecting tunnel junction were grown entirely by MO-CVD techniques and which exhibited voltage addition ($V_{OC} \approx 2.1V$) under illumination. This achievement together with other results of significance obtained in the Phase 1 program are summarized in this section. A more detailed task-by-task summary is given in Section 3, and full details of the investigations are given in Section 2.

The program was conducted for the purpose of developing the technologies necessary for fabricating stacked multiple-bandgap solar cell assemblies having AM0 1-sun efficiencies of 25 percent or greater at 25°C. The terms of the contract required that four different semiconductor material combinations judged feasible for use in fabricating SMBSC structures be investigated, so that a material combination and its associated processing technologies could be selected at the end of the 14-month program for use in fabricating 100 2 cm x 2 cm cell assemblies for delivery at the conclusion of the 24-month two-phase contract.

Accordingly, investigations were undertaken on the following SMBSC materials systems, all of which involve the GaAℓAs-GaAs system as the basic building block: 1) the two-cell GaAs-Ge structure, made by MO-CVD and conventional CVD techniques; 2) the two-cell GaAs-InGaAs structure, using LPE methods; 3) the three-cell GaAℓAs-GaAs-GaAsSb structure, employing MO-CVD methods; and 4) the three-cell GaAℓAs-GaAs-InGaAsP structure, involving LPE methods.

After the program was under way, MBE techniques were incorporated into the investigations of structures 1, 3, and 4 by mutual agreement of the Air Force and Rockwell. Late in the program, with three months of Phase 1 remaining, a change in program emphasis was introduced by the Air Force to limit the investigations to GaAℓAs-GaAs and GaAs-Ge two-cell structures and the possible GaAℓAs-GaAs-Ge three-cell assembly that might also result. Primary emphasis was to be on the MO-CVD technique, supplemented – when appropriate – by MBE, LPE, or other deposition and/or processing methods.

The best results were achieved with the two-cell GaAℓAs-GaAs structure made entirely by MO-CVD, although similar structures made by a combination of MO-CVD and MBE techniques appeared quite promising. Two-cell GaAs-Ge assemblies, made by a combination of MO-CVD and conventional CVD methods or by combined MO-CVD and MBE techniques, were not as successful, although theoretically capable of essentially the same overall efficiency (up to ~25 percent) as the GaAℓAs-GaAs tandem structure. No attempt was made during the Phase 1 program to prepare a three-cell GaAℓAs-GaAs-Ge stacked assembly. The other materials combinations included in the original program received considerably less attention during the investigations, and correspondingly less progress toward the program goals was made with those structures.

The investigation of the three-cell GaAℓAs-GaAs-GaAsSb tandem structure received major program emphasis, and within that investigation, the GaAℓAs-GaAs two-cell SMBSC was extensively developed. Although exclusively MO-CVD techniques were originally expected to be involved, MBE methods were also applied beginning part way through the program. The principal developments required were satisfactory GaAℓAs large-bandgap (1.8-2.0 eV) cells and conducting (presumably tunneling) junctions in GaAℓAs and/or GaAs (with the former preferred) to provide the non-rectifying connecting layer between cells of the SMBSC. The GaAsSb materials system was investigated briefly using LPE techniques (see below), but MO-CVD studies with these materials had not been undertaken prior to the time at which the program emphasis was changed.

Window-type alloy cell structures were grown by MO-CVD on n^+GaAs:Si and n^+GaAs:Te substrates with typical configurations $pGa_{1-y}Al_yAs/pGa_{1-y}Al_xAs/nGa_{1-x}Al_xAs$ ($y \geq 0.8$, $x = 0.2$-0.4), in some cases with a thin p^+GaAs:Zn cap layer on top to facilitate contacting the p layer of the cell. Deposition temperatures ranged from 700 to 800°C, with 750°C the most common. Most cells were 0.5 cm x 0.5 cm, although small mesa cells were processed in some cases.

Cell response appeared to improve generally with increasing deposition temperature, and active layer compositions of $x = 0.24$-0.30 seemed preferable. The best cell parameters observed were in a structure grown at ~750°C with $y = 0.8$ and

$x = 0.24$: $V_{OC} = 0.96V$, $J_{SC} = 12.0$ mA/cm^2, fill factor = 0.63, and $\eta = 5.4$ percent (AM0, no AR coating). Spectral response measurements showed that reduced short-wavelength response was the cause of the relatively small J_{SC} values obtained, and it appeared that poor current collection efficiency (i.e., short minority-carrier diffusion lengths) in the p-type junction layer most likely caused the reduced short-wavelength response.

Further studies of a variety of alloy cell configurations indicated that, although V_{OC} increased as the Aℓ content of the junction layer increased, the V_{OC} values were always appreciably less than theoretically expected values except for very low Aℓ content ($x < 0.10$); highest V_{OC} values found were ~1.1V for cells with $x = 0.35$. The J_{SC} values were found to depend on Aℓ content and thickness of the window layer as well as the junction layers. Junction depths < 0.7 μm were clearly preferred, with thicker layers causing reductions in J_{SC} – consistent with minority-carrier diffusion lengths ≤ 0.5 μm. Window layer compositions with $y = 0.9$ allowed better blue response and higher J_{SC} values than those with $y = 0.8$, and window layer thicknesses ≤800Å were preferred.

Most cells had J_{SC} values < 6 mA/cm^2 (AM0, no AR coating) irrespective of design; fill factors typically ranged from 0.60 to 0.76 and efficiencies were generally ≤ 4 percent (AM0, no AR coating). Thus, as of the end of the Phase 1 program the performance of the GaAℓAs cells still requires considerable improvement, so continued emphasis is expected in Phase 2.

Several attempts were made to achieve tunneling properties in GaAℓAs junction structures grown by MO-CVD, beginning early in the program. Both n^+/p^+ and p^+/n^+ junction structures with $Ga_{1-y}Aℓ_yAs$ compositions of $y = 0.08$ to $y = 0.37$ were grown at temperatures of 700 and 750°C, but at best only weak tunneling was observed. Although the emphasis in the remainder of Phase 1 was on tunnel junction structures in GaAs (see below), it is expected that further effort will be devoted to achieving tunneling structures in the alloy in the Phase 2 program since that configuration is preferred in terms of overall performance of the stacked assemblies.

Good tunnel-junction intercell connecting structures were made in GaAs by both MO-CVD and MBE techniques. Both n^+/p^+ and p^+/n^+ structures were made by MO-CVD at temperatures from 630 to 750°C, with better results obtained at ≤ 650°C, as shown in Figure 3. Very high (essentially ohmic) junction conductivity was achieved in some of the structures – especially in n^+/p^+ structures – more than adequate for use as an intercell connection under 1-sun AM0 conditions. Preliminary annealing tests indicated that the tunneling characteristics might not survive subsequent elevated temperature processing required for growth of the top cell in a stacked assembly because of diffusion of the Zn dopant in the p^+GaAs, but n^+/p^+ structures grown in GaAs at 630°C were used in the first successful two-cell GaAℓAs-GaAs SMBSC described below. However, the still-open question about the consistent stability of these structures at high temperatures requires further investigation in the Phase 2 program.

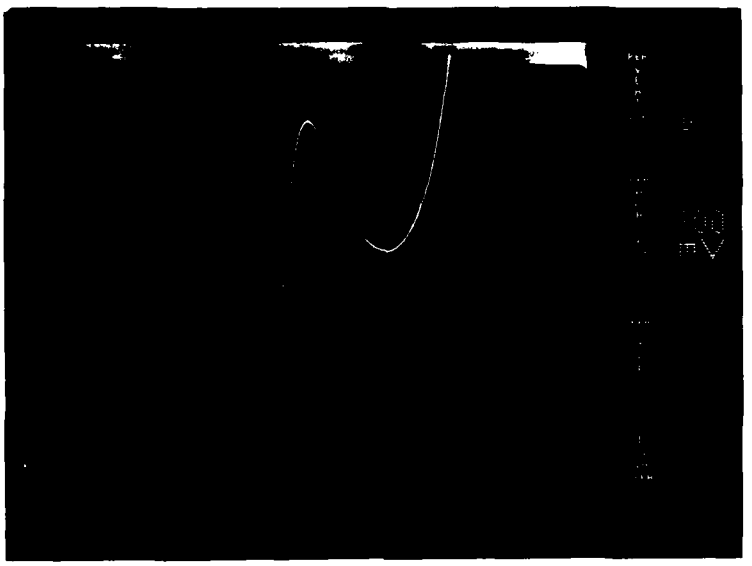


Figure 3. Tunneling I-V Characteristic for 25x25 mil Mesa Diode in p^+GaAs:Zn/n^+GaAs:Se Epitaxial Structure Grown by MO-CVD on nGaAs:Si Substrate at 650°C.

An alternative solution was provided by the use of p^+GaAs layers grown by MBE and doped with Be, a slow-diffusing impurity. A hybrid n^+/p^+ tunnel junction structure, involving n^+GaAs:Se grown by MO-CVD at 630°C and p^+GaAs:Be formed by MBE on a GaAs:Cr substrate exhibited reasonable tunneling properties, and all-MBE structures consisting of n^+GaAs:Sn/p^+GaAs:Be deposited at ~540°C exhibited essentially ohmic conducting behavior. Both structures appeared to maintain tunneling properties after high-temperature cycling typical of that required for growth of the top cell in a stacked assembly.

GaAs heteroface cells were made by both MO-CVD and MBE techniques. The cells made by MO-CVD on GaAs substrates early in the program were not up to previous performance standards, but results gradually improved to the point that cells with $V_{OC} = 0.97V$, $J_{SC} = 20$ mA/cm^2, fill factor ≈ 0.8, and $\eta = 11.5$ percent (AM0, no AR coating) were being made. A very high degree of uniformity of cell performance over the area of 2 cm x 4 cm substrates was realized, demonstrating one of the major strengths of the MO-CVD process. Deposition temperatures of 700-750°C, window layer thicknesses of 500-800Å, and p-layer thicknesses ≤ 0.75 μm were found preferable. Heteroface cells made by MBE on GaAs substrates were of generally good quality, the best results being $V_{OC} = 0.94V$, $J_{SC} = 17.2$ mA/cm^2, fill factor = 0.84, and $\eta = 10.1$ percent (AM0, no AR coating). Relatively little development effort was expended on the MBE-grown GaAs cells, however.

Two-cell GaAlAs-GaAs SMBSC's were fabricated and tested approximately midway through the program, as soon as evidence of tunneling in n^+/p^+ structures in GaAs had been observed. Although the structures were made with the connecting n^+/p^+ junction structure both in GaAs and in GaAlAs, only the former exhibited adequate tunneling properties. The successful configuration was GaAlAs cell/ GaAs n^+-p^+ junction/GaAs cell grown by MO-CVD on an nGaAs:Si substrate. Best results were obtained with the structure shown in Figure 4. Growth temperatures were 750, 630, and 700°C for the alloy cell, the tunneling junction, and the GaAs cell, respectively.

Under tungsten lamp illumination this SMBSC exhibited a V_{oc} of ~2.1V and a J_{sc} of ~4.5 mA/cm^2; the I-V curves are shown in Figure 5. This represents the first successful achievement of a stacked cell grown completely by a vapor-phase process and exhibiting voltage addition. The V_{oc} value is believed to be the highest achieved up to that time for a stacked cell grown by any process. It appeared that the $Ga_{0.7}Al_{0.3}As$ cell in this structure was probably the limiting component in the performance of the stacked assembly, preventing higher photocurrents from being collected and thus better overall performance from being achieved.

At the end of Phase 1 several additional two-cell GaAlAs-GaAs SMBSC's were prepared with the alloy cell grown at higher temperatures (775 and 800°C) and others grown at 750°C but with greatly reduced thicknesses (~100Å) in each of the tunnel junction layers. The intended improvements were not achieved, however, so work with the GaAlAs-GaAs tandem structure must be continued into Phase 2 in order to realize the expected performance with this materials combination.

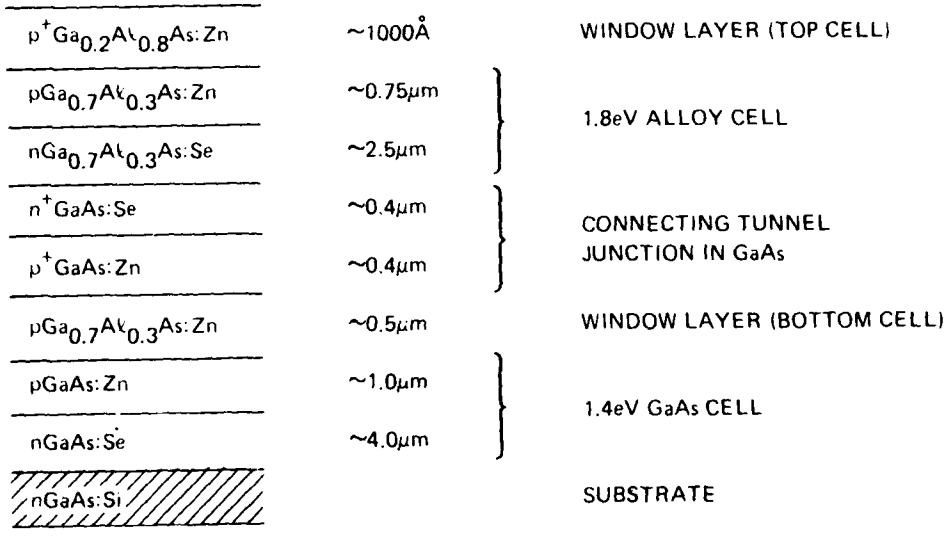


Figure 4. Configuration of Two-cell GaAlAs-GaAs SMBSC for which Voltage Addition was Observed under Illumination

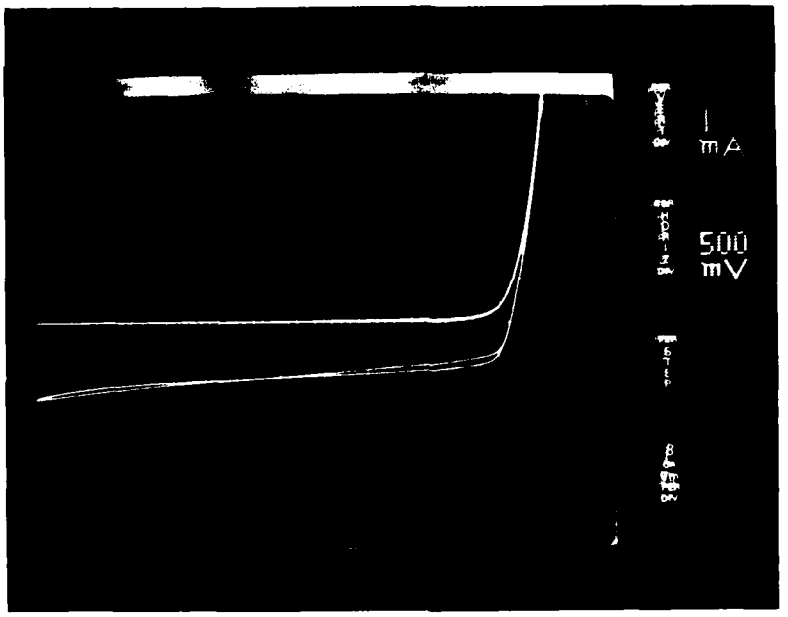


Figure 5. Dark and Illuminated (microscope lamp) I-V Curves for Two-cell SMBSC Grown Entirely by MO-CVD on GaAs:Si Substrate, with $Ga_{0.7}A_{0.3}As$ Cell and GaAs Cell Connected by Intermediate n^+-p^+ Junction in GaAs.

Considerable attention was also given the two-cell GaAs-Ge SMBSC structure, the GaAs heteroface cells again to be made by MO-CVD and MBE techniques, Ge cells by CVD and MBE techniques, and connecting tunnel-junction structures in GaAs by MO-CVD and MBE, both singly and in combination. Two possible SMBSC configurations were considered, one involving an n^+GaAs substrate and the other involving an n^+Ge substrate, with the latter being preferred and thus receiving the major emphasis. Combining of the individual components into a functioning two-cell stacked assembly was accomplished later in Phase 1, but performance characteristics were not fully established.

The status of GaAs heteroface cell growth on GaAs substrates is discussed above. It was found that GaAs heteroface cells grown by MO-CVD on Ge substrates, however, had higher leakage currents, reduced J_{sc} values, generally poorer photovoltaic performance, and less uniformity of cell properties over the area of a large substrate, even when the Ge substrate was covered with ~1000Å of SiO_2 to reduce interactions. Best cell properties were typically V_{oc} = 0.96-0.98, J_{sc} = 16-17 mA/cm^2, fill factor = 0.70-0.75, and η = 8-9 percent (AM0, no AR coating). There was some evidence that a non-standard pre-deposition procedure, involving Ge substrate exposure to AsH_3 for only a few seconds before GaAs deposition commenced, produced a less defective interface region and somewhat better

cell performance. Modifications in cell layer dimensions and doping impurity concentrations and improved Ge substrate quality are expected to result in considerably better GaAs cell performance in future work with this material combination.

In addition to the heteroface GaAs cells grown by MBE on GaAs substrates (mentioned above), junction structures were also grown on Ge substrates by this technique. Although the layers were of high quality it appeared that heterojunctions had also been formed, unintentionally, at the GaAs-Ge interface. Since relatively little effort was devoted to MBE-grown GaAs cells on either GaAs or Ge substrates in Phase 1, the work is expected to be expanded in the Phase 2 program.

Ge solar cells were made by both CVD (GeH_4 pyrolysis in H_2) and MBE techniques; some limited investigations were also conducted with spin-on oxide impurity sources for producing diffused junction structures. Most of the cells were prepared on Ge substrates, that being the preferred configuration for the SMBSC. Best CVD quality was obtained at the upper end of the useful deposition temperature range (~800°C) and with relatively high deposition rates (~0.7 μm/min). However, substrate stability can become a problem during long depositions at such temperatures. The best CVD cell parameters, obtained with B-doped p layers and undoped n-type layers on nGe substrates, were V_{OC} = 190-200 mV, J_{SC} = 31-33 mA/cm^2, fill factor = 0.65, and η = ~3 percent (AM0, no AR coating). Much improved results are expected with changes in cell layer thicknesses and doping concentrations (especially the n layers) and in the cell contacting procedures; these changes are planned for the Phase 2 program.

Ge cell structures were also made by MBE techniques, by depositing a layer of As on p-type (100)Ge and subsequently diffusing the As into the Ge in situ at appropriate temperatures. The resulting diffused-junction cells were not as good as those made by CVD but were adequate for use in preparing experimental stacked GaAs-Ge SMBSC structures using exclusively MBE techniques.

Experimental two-cell GaAs-Ge stacked assemblies were made entirely by MBE techniques and by combined MO-CVD and MBE, late in the program. The all-MBE structure appeared to contain a double heterojunction rather than the intended structure; the hybrid structure, which involved an MO-CVD heteroface GaAs cell grown at 750°C on an n^+/p^+ GaAs tunnel junction structure grown by MO-CVD at 630°C on a diffused Ge cell structure formed by MBE techniques, was not fully processed and evaluated prior to the end of the program. It is expected that additional GaAs-Ge SMBSC's prepared by various combinations of CVD and MBE techniques will be investigated in Phase 2.

Investigation of the two-cell GaAs-InGaAs SMBSC, to be prepared by LPE methods on n^+GaAs substrates, involved mainly the experimental growth of InP layers on GaAs substrates (to provide the lattice-matched window for the InGaAs cell) and of InGaAs layers on InP, in addition to an evaluation of AlGaAsSb as an alternative materials system to InGaAs for the low-bandgap cell.

The LPE growth of p^+InP layers on n^+GaAs substrates from both In and Sn solvents was only partially successful. Acceptable growth on (111B)GaAs was achieved with In solvent in a narrow temperature range around 520°C, and marginally

acceptable growth on (100)GaAs was obtained with Sn solvent at higher temperatures provided that large vertical temperature gradients were maintained across the liquid-solid growth interface to minimize etch-back. However, high densities of inclusions persisted at the interface, so these structures were not satisfactory for stacked cell configurations. Consequently, InP layers grown on GaAs substrates by MO-CVD were separately prepared for the subsequent LPE growth experiments with InGaAs.

Initial LPE growth experiments with the InGaAs composition lattice-matched to InP were done with single-crystal (111B)InP substrates. Junction structures of pInGaAs:Zn/nInGaAs (undoped) were grown, and despite some problems in making ohmic contacts cell structures were fabricated and characterized; low current collection efficiency, junction movement due to Zn diffusion, and possible formation of an InP-InGaAs heterojunction resulted in generally poor performance. When thicker undoped single layers were grown at lower temperatures (~630°C), with slight substrate etchback allowed prior to growth, an n-type layer of composition $In_{0.53}Ga_{0.47}As$ ($E_g \approx 0.7$ eV) resulted and a junction was formed in it by Zn out-diffusion from the p^+ substrate.

Solar cells exhibited V_{OC} values <0.1V and J_{SC} values of ~16 mA/cm^2 (AM1, no AR coating). The low V_{OC} values were attributed to large reverse saturation currents and poor diode factors, and there was again some indication of a possible heterojunction at the InP-InGaAs interface. Subsequent preliminary experiments with the MO-CVD InP/GaAs composite substrates resulted in discontinuous layers and poor melt wipeoff, but the experiments were not continued because of the change in program emphasis that became effective at that time.

Some attention was also given to AlGaAsSb as an alternative small-bandgap cell material. Window-type cell structures were grown on n-type single-crystal GaSb substrates by LPE with the configuration $pGa_{0.7}Al_{0.3}AsSb$/pGaSb (undoped)/nGaSb (substrate), but poor photovoltaic properties (especially fill factor and short-wavelength response) were obtained. Modified structures, with improved contacts to reduce series resistance and thinner pGaSb layers to improve short-wavelength response, were then prepared with the configuration $p^+Ga_{0.7}Al_{0.3}AsSb$/$pGa_{0.9}Al_{0.1}Sb$/nGaSb (substrate). Addition of Al to the GaSb p layer reduced the layer growth rate, so that shorter deposition times (~1 min at ~520°C) permitted growth of p layers that were 2-3 μm thick.

These changes allowed attainment of cells with the parameters $V_{OC} = 0.240$V, $J_{SC} = 29$ mA/cm^2, fill factor = 0.51, and $\eta \approx 3.5$ percent (AM1, no AR coating). Junction leakage and series resistance remained as problems, but the results were sufficiently encouraging to prompt a brief investigation of various contact materials for both p-type and n-type GaSb to attempt to reduce series resistances losses. Pure Au contacts were found best for both conductivity types. Several additional cell structures, including some with higher Al composition (~0.7) in the window layer, were subsequently prepared, but the investigations were not carried further.

The study of the three-cell LPE-grown GaAlAs-GaAs-InGaAsP SMBSC assembly using n^+GaAs single-crystal substrates involved two main areas of investigation – LPE growth of 2.0 eV GaAlAs cell structures on GaAs surfaces and LPE growth

of 1.0 eV InGaAsP layers. Existing well-established methods for LPE growth of GaAs cells provided the third major cell technology needed for this SMBSC. The GaAs (or GaAlAs) tunnel junctions and InP/GaAs tunneling heterojunctions made by either LPE or MBE techniques would provide the needed cell interconnections.

Window-type alloy cell structures were grown by LPE on n^+GaAs substrates with the configuration $p^+Ga_{0.1}Al_{0.9}As/pGa_{0.7}Al_{0.3}As/nGa_{0.7}Al_{0.3}As$. Some experimental n^+/p^+ alloy structures were also grown, but incomplete wipeoff in the LPE boat resulted in cross-contamination of the melts and unsatisfactory structures. A special LPE boat was then designed, and fabrication was completed by an outside vendor several months later. Modified LPE growth procedures were developed for use with the new boat, and several types of alloy cell structures were prepared.

Complete small-area window-type cells were fabricated both by conventional processing and by processing that involved Zn diffusion into the window layer. Window-layer Al contents were in the range y = 0.8-0.9 and junction layer Al contents x = 0.2-0.4. The cells generally had good fill factors (typically 0.7-0.8) but relatively low V_{OC} and J_{SC} values. Spectral response curves showed poor utilization of the short-wavelength illumination, indicating needed changes in window layer thickness and junction layer thickness and Al content.

Some additional alloy cells were prepared near the end of Phase 1, including several in which only a p-type active layer and a p-type window layer were deposited in succession by LPE on an n^+GaAs substrate, followed by Zn diffusion through the window layer and the p layer to produce the active p-n junction just inside the substrate. However, it was found difficult to control the diffused junction depth. The cells grown and processed by conventional procedures were somewhat better; J_{SC} values up to 8.5 mA/cm^2 and efficiencies up to 4.6 percent (AM0, no AR coating) were obtained. Open-circuit voltages (~1.0V) and fill factors (~0.75) were about the same for both types of cell.

Limited investigation of the LPE growth of InGaAsP for the 1.0 eV bandgap cell was also undertaken. Multilayer structures of the configuration pInP/pInGaAsP/nInGaAsP/nInP were grown on n^+InP substrates. Analysis showed the quaternary layers had the composition $In_{0.75}Ga_{0.25}As_{0.5}P_{0.5}$, indicating a bandgap of ~1 eV and a lattice match to InP, but photoresponse measurements showed cutoff at the InP band edge. This was believed caused by Zn dopant diffusion from the two upper layers into the nInP buffer layer, shifting the active junction to that location. The study of this quaternary was not carried further in Phase 1.

Cell modeling and analysis studies in the Phase 1 program showed that only limited response is achievable for a Ge cell in the wavelength region beyond the direct bandgap ($\lambda > 1.5$ μm), even for a thick wafer-based cell, but that use of a back-surface field considerably enhances the response of a thin (i.e., all deposited film) cell in the region $0.9 \leq \lambda \leq 1.5$ μm.

The studies also led to estimates of ~0.5 μm for the minority-carrier diffusion lengths in the p-type junction layers of heteroface GaAlAs alloy cells, through comparison of modeled spectral photoresponse with experimentally determined

responses of MO-CVD and LPE cell structures. Similar matching of modeled and measured spectral photoresponses for thin-window GaAs cells, especially those made by MBE techniques, was undertaken and led to the conclusion that specific reflectivity measurements must be made for GaAs cells having GaAlAs window layers if correct internal photoresponse curves are to be obtained.

Analytical techniques were also applied to the development of an algorithm that provides the design parameters for n-layer ($n \geq 3$) antireflection coatings for use on SMBSC assemblies, which have spectral ranges broader than those of any of the component cells involved. Three-layer coating designs for two-, three-, and four-cell assemblies were developed using MgF_2 or CaF_2 for the top layer, SiO_2 for the middle layer, and Ta_2O_5 or TiO_2 for the bottom layer. No experimental development of the coatings was undertaken in Phase 1, however.

2. DETAILED DISCUSSION OF RESULTS

This section contains detailed descriptions of the technical activities and the results achieved during the 14-month Phase 1 program. The discussion is arranged in order by technical task, with one exception noted below.

Pursuit of the Phase 1 program objectives specified in Section 1.2 was accomplished by means of seven main technical tasks, as follows:

1. SMBSC Modeling and Analysis
2. GaAs-Ge SMBSC Technology Development
3. GaAs-InGaAs SMBSC Technology Development
4. GaAlAs (2.0eV)-GaAs-GaAsSb SMBSC Technology Development
5. GaAlAs (2.0eV)-GaAs-InGaAsP SMBSC Technology Development
6. Characterization of Materials and Photovoltaic Devices
7. Development of AR Coating Technology.

The work of the first six tasks was planned to begin in the first month of the contract; the activity of Task 7 was scheduled to commence in the seventh month of the program.

Task 1 and Task 7 were carried out primarily at the Rockwell Thousand Oaks laboratories. Tasks 3 and 5 were planned to involve application of LPE techniques and thus were also pursued at the Thousand Oaks facility.

Tasks 2 and 4 involved use of the MO-CVD technique and thus were centered at the Anaheim laboratories of the Rockwell Electronics Research Center. The materials and device characterization work of Task 6 was carried out at both laboratories throughout the Phase 1 program.

Following a contract program progress review meeting held at the end of the eleventh month of the contract a change in program emphasis was agreed upon for the remaining three months of Phase 1. Experimental results achieved in the program up to that time, as well as related experimental results being achieved in other programs at Rockwell at the same time, prompted the following modified approach for Phase 1:

1. The program effort was to be limited to GaAlAs-GaAs, GaAs-Ge, and GaAlAs-GaAs-Ge stacked multiple-bandgap solar cell systems.
2. There was to be greatly increased emphasis on the MO-CVD technique for making these structures.

3. Other deposition and processing techniques were to be used in certain hybrid combinations to augment CVD when it appeared that doing so would improve the chances of achieving the program goals; those other techniques might include LPE, molecular beam epitaxy (MBE), thermal diffusion, or ion implantation.

Thus, effective at the start of the twelfth month of the Phase 1 program the contract work emphasized only the GaAlAs-GaAs-Ge materials system and the two-cell and three-cell stacked assemblies that can be made in that system. The emphasis was on use of CVD techniques, especially MO-CVD, although other growth and processing methods (LPE, MBE) were utilized to supplement the CVD methods.

The activities and the results associated with these tasks are described in the following discussions, arranged by task except for the work of Task 6 (Characterization of Materials and Photovoltaic Devices), which is included as appropriate in the other task discussions.

2.1 SMBSC MODELING AND ANALYSIS

Because of the complexity of SMBSC structures and the fact that there was little experimental information prior to the start of this program on the behavior of individual solar cells used in monolithic tandem assemblies, it was very important to provide some guidance for the experimental investigations by means of analytical modeling of the structures involved.

Considerable previous work had been done at Rockwell on the modeling of GaAs solar cell performance both for normal one-sun illumination intensities and for high-concentration (multiple-sun) illumination conditions. Those analyses utilized theoretical expressions that were strengthened with actual cell performance parameters obtained with a variety of experimental cell structures.

The requirement that the individual cells connected in tandem in the SMBSC structure must share a common current – that is, that the photogenerated current of each cell at its operating point when used in the stacked assembly must match that of every other cell in the SMBSC – places very stringent limitations on the composition, the design, and the photovoltaic properties of these cells. This makes it essential to understand and control the properties of the individual cells in detail. Accurate analytical modeling of both individual and stacked cell performance can assist in achieving this needed understanding and control, and can often prevent the conduct of unnecessary or superficial experiments and provide guidance to the really essential ones.

Similarly, the AR coating requirements of a tandem cell assembly will be different from those of, for example, the uppermost cell in the stack if it were used individually in its more restricted spectral range. Analytical modeling can provide the data required to develop a satisfactory broad-band AR coating for SMBSC structures of various configurations.

Thus, this task was to include the generation of refinements in the existing model used at Rockwell for solar cell performance analysis, incorporating experimental data on the I-V characteristics of various photovoltaic junctions as well as nonrectifying junctions. Application of the improved model was expected to lead

to identification of candidate two-cell, three-cell, and four-cell SMBSC combinations potentially useful and feasible for experimental studies. Calculations were also to be made for the purpose of determining optimum materials properties, such as doping levels and alloy compositions, and optimum physical design parameters, such as electrical contacts and AR coatings, for the candidate SMBSC systems of interest. The results of the modeling calculations were expected to strongly influence the experimental program; it was intended that considerable mutual interaction between this task and the experimental investigations would occur, particularly during the first six months of the program.

2.1.1 Multilayer AR Coating Design

One of the first problems to be examined in this task was that of AR coating designs for SMBSC assemblies. Although the development of suitable AR coating technologies would be done under Task 7 (Section 2.6) the necessary modeling and analysis for such development is part of this task.

The SMBSC structure requires the suppression of reflection from the surface over a broad spectral range. The number of dielectric layers required and their composition and thickness will depend on the cell material in the top layer and the spectral bandwidth to be covered. For a two-cell system with GaAs as the top layer the spectral bandwidth is 0.3-1.8μm. For a three-cell system with GaAℓAs or GaInP as the top cell material the spectral bandwidth is 0.3-1.2μm, and for a four-cell system with GaAℓAs or GaInP as the top cell material the bandwidth is again 0.3-1.8μr

Because of the different optical reflectivity vs wavelength characteristics for a given thin-film material when used in a stacked multilayer assembly relative to its characteristics when used alone or on a substrate of identical composition it was necessary to reevaluate the requirements for AR coatings for the materials used in the SMBSC structures being developed in this program. Consequently, preliminary consideration was given to those requirements by means of modeling analysis of a two-layer AR coating for a GaAs surface over the broader wavelength band of importance for a SMBSC, namely, the range from ~0.3μm to ~1.8μm.

Attempts to extend the wavelength range of coverage of the existing two-layer algorithm suggested that the covered spectral band could probably be expanded to the interval 0.5-1.7μm wavelengths with less than 10 percent reflection at any one wavelength and about 6 percent average loss throughout the band, with a high-reflectivity (~13 percent) peak near the center of the band (at ~1.15μm). However, the reflection loss outside this band was found to be considerably higher, with an especially steep increase in the reflectivity at the short-wavelength end of the band. The preliminary calculations indicated that three or more layers would probably overcome this problem, so attention was directed to development of an algorithm for a multilayer AR coating of n layers, with n≥3.

The resulting algorithm can be used with a given set of constraints to optimize the values of independent variables using a generalized technique (Ref 7). In this program it was used to optimize a three-layer AR coating design. The materials considered for the three layers were restricted to those commonly used for AR coatings and readily handled experimentally – MgF_2 or CaF_2 for the top layer, SiO_2 for the middle layer, and Ta_2O_5 or TiO_2 for the bottom layer (next to the solar cell).

Figure 6 shows the calculated reflection loss as a function of wavelength for a three-layer design optimized for 0.3 to 1.1μm operation (three-cell system). The average reflection loss for this case comes out to be 3.6 percent. Figure 7 shows a simular result for 0.3 to 1.8μm operation (two- or four-cell system). In this case, the average reflection loss comes out to be 5.4 percent. In both instances the optimization was for minimum integrated reflection loss over the specified spectral band.

In practice, however, it is necessary to optimize the short-circuit current or, more accurately, the current at maximum power of the cell assembly. This depends on the solar spectrum and the internal collection efficiencies of the solar cells. When a simplified model for the cell collection efficiency was used with the AM0 spectral distribution, the optimized AR-coating design for the 0.3 to 1.8μm range (i.e., for two or four cells in the stack) came out as shown in Figure 8. The overall reflection loss in this case reduces the short-circuit current of the cell assembly by only 3.8 percent. It should be noted that the peak reflection loss in Figure 8 occurs near 0.4μm wavelength, while that in Figure 7 is at $\sim$0.7μm, so the design of Figure 8 is a better match to the AM0 spectrum.

These results demonstrate the power of the algorithm developed for obtaining optimum AR coating designs. Final design calculations can be performed whenever the other pertinent experimental data on individual cell performances become available later in the program.

2.1.2 Ge Solar Cells

Early in the program some preliminary calculations were carried out for Ge solar cells to assist in determination of the required device parameters for the 0.7eV cell to be used in the two-cell GaAs-Ge SMBSC to be made by MO-CVD in Task 2.

The computer-plotted data of Figure 9 show calculated internal spectral response curves for Ge p-n junction cells with (solid curve A) and without (solid curve B) a back-surface field (BSF) created by the presence of an n^+-n junction at the back of the wafer-based cell structure. The specific device parameters used in the calculations were as follows, with t = thickness, L = minority carrier diffusion length, and s = surface recombination velocity:

Cell configuration (all Ge): $p^{++}/p^+/n/n^+$

Characteristics of individual regions:	p^{++}	t = 500 Å, L_n = 5μm, s = 10^6 cm/sec
	p^+	t = 1μm, L_n = 50μm, s_i = 10^4 cm/sec
	n	t = 300μm
	Substrate	L_p = 100 m, s_b = 100 cm/sec for BSF case and 10^5 cm/sec for ohmic contact case

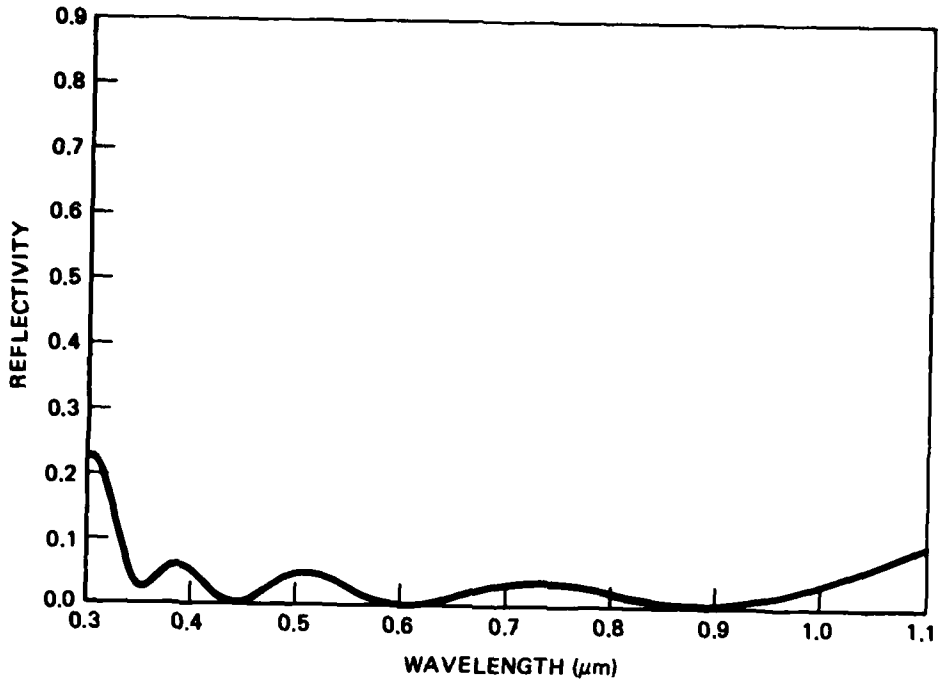


Figure 6. Optimized 3-layer AR Coating Design For AM0 Spectrum with 4062A CaF_2 Top Layer, 838A SiO_2 Middle Layer, and 591A TiO_2 Bottom Layer for 0.3-1.1μm Operation (3-cell SMBSC) and Minimum Integrated Reflection Loss

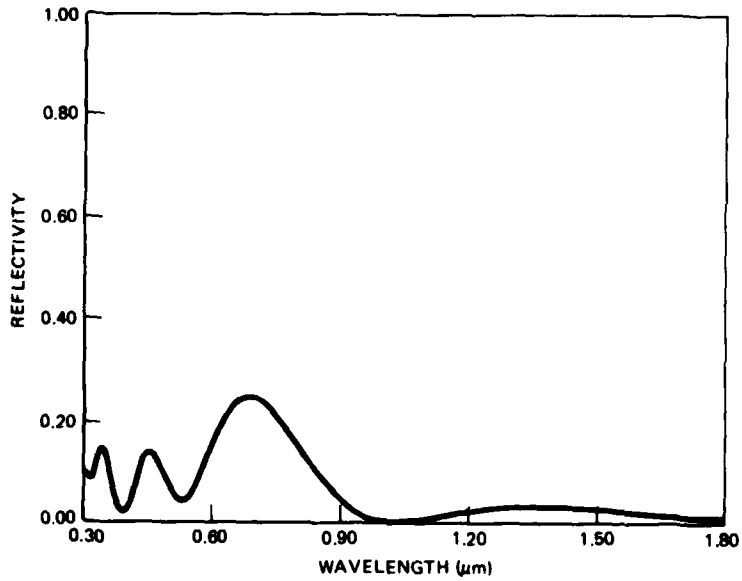


Figure 7. Optimized 3-layer AR Coating For AM0 Spectrum with 1810A MgF_2 Top Layer, 919A SiO_2 Middle Layer, and 1296A TiO_2 Bottom Layer, for 0.3-1.8μm Operation (2-cell or 4-cell SMBSC) and Minimum Integrated Reflection Loss

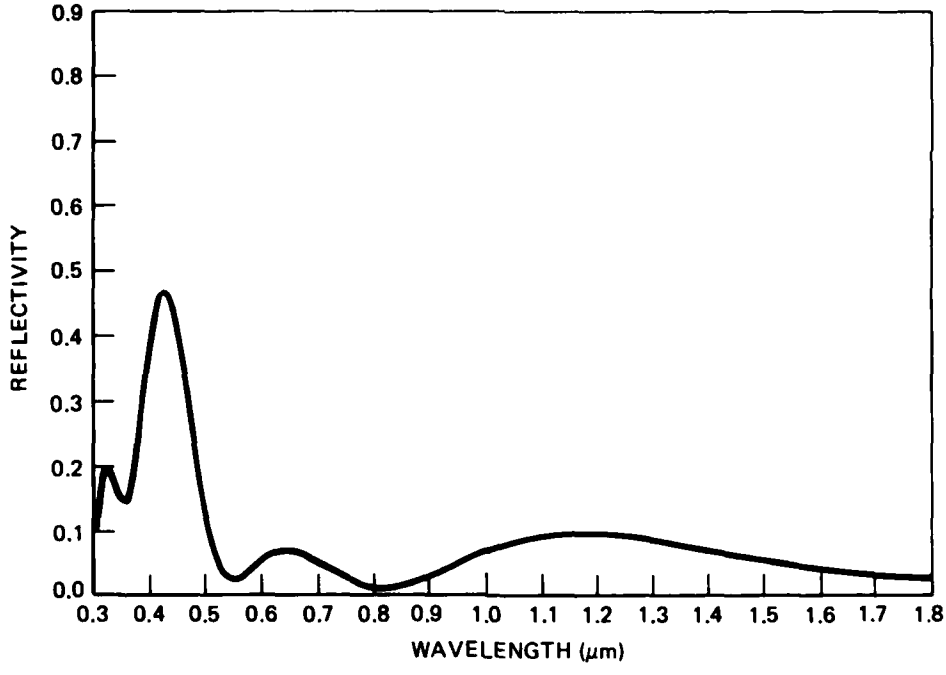


Figure 8. Optimized 3-layer AR Coating Design for AM0 Spectrum with 1756Å MgF_2 Top Layer, 1340Å SiO_2 Middle Layer, and 835Å Ta_2O_5 Bottom Layer, for 0.3-1.8μm Operation (2-cell or 4-cell SMBSC) and Maximum Short-circuit Current for Cell Assembly

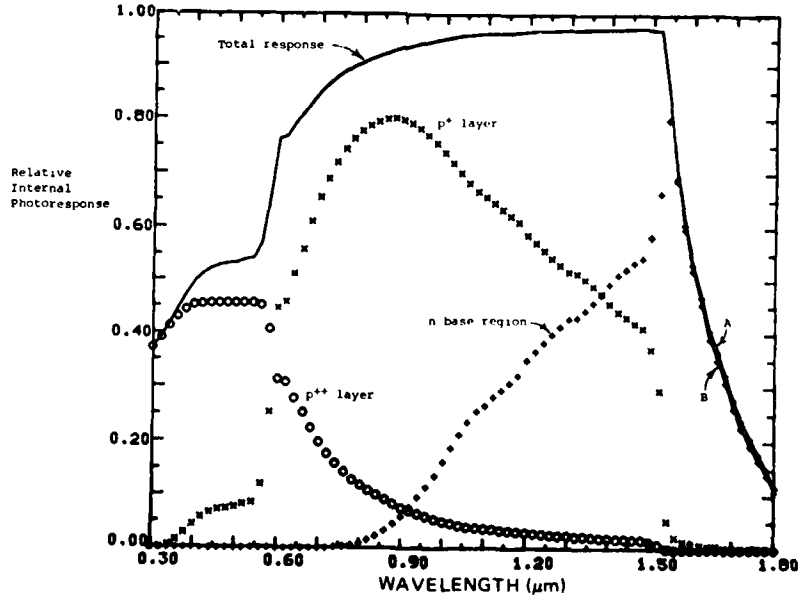


Figure 9. Calculated Internal Photoresponse (charge collection efficiency) for Ge Solar Cell of Specified Parameters

The calculated spectral response data for the individual layers of this cell structure are also shown in the figure as plotted data points. It can be seen that even with a base region (substrate wafer) that is 300μm thick the cell response for energies below the Ge direct bandgap (wavelengths greater than ~1.5μm) decreases quite rapidly. Furthermore, the back-surface field does not increase the long-wavelength response very much because of the very limited optical absorption in the region of the indirect bandgap. To collect photocurrent efficiently at wavelengths beyond 1.5μm and up to about 1.8μm (corresponding to the indirect bandgap of Ge) very thick Ge substrates would be required, and not much help would be obtained from the back-surface field. However, such a back-surface field can be used to advantage to enhance photocurrent collection in very thin Ge cells in the region out to the direct-gap wavelength of 1.5μm. This would be a significant improvement for a thin Ge cell made by an epitaxial growth process on, for example, a GaAs substrate wafer. (See Section 2.2.)

The calculated spectral response curves for a thin epitaxial Ge cell (~6μm thickness) with and without the back-surface field from an n-n^+ back junction are shown in Figure 10. The device parameters used in these calculations were as follows:

Cell configuration $p^{++}/p^+/n$
($p^{++}/p^+/n/n^+$ with back junction)

p^{++} region: $t = 500\text{Å}$, $L_n = 5\mu m$, $s = 10^6$ cm/sec

p^+ region: $t = 1\mu m$, $L_n = 50\mu m$, $s = 10^4$ cm/sec

n region: $t = 5\mu m$, $L_p = 100\mu m$, $s = 10^5$ cm/sec for ohmic contact case
$= 100$ cm/sec for BSF case

A distinct improvement in spectral response between 0.9 and 1.5μm is seen to result from the presence of the back-surface field, which was assumed for this calculation to result in a surface recombination velocity at the back surface of 100 cm/sec. The back-surface recombination velocity can be related to the device parameters through the following expression:

$$s_{nn^+} = \frac{D_{pn^+}N_n}{L_{pn^+}N_{n^+}} \coth \frac{w_{n^+}}{L_{pn^+}},$$

where s_{nn^+} is the n-n^+ interface recombination velocity, D_{pn^+} is the diffusion constant for holes in the n^+ region, N_n is the electron concentration in the n region, L_{pn^+} is the hole diffusion length in the n^+ region, N_{n^+} is the electron concentration in the n^+ region, and w_{n^+} is the thickness of the n^+ region. From this expression suitable device parameters can be selected to result in a value of 100 cm/sec for the surface recombination velocity.

An epitaxial Ge cell of such dimensions could be used as part of the two-cell GaAs-Ge SMBSC configuration being developed in Task 2. The accuracy of the Ge cell model can be further improved when experimental data on Ge cells fabricated in the Task 2 effort become available and are incorporated into the model.

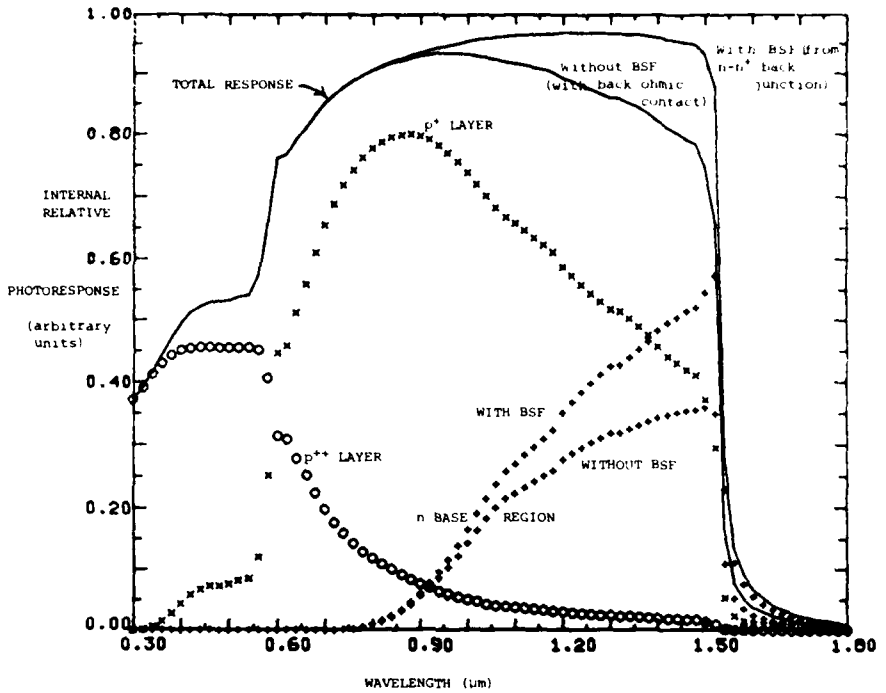


Figure 10. Calculated Internal Photoresponse (*charge collection efficiency*) for Thin Ge Solar Cell with and without Back-surface Field Associated with $n\text{-}n^+$ Junction at Back of Cell

2.1.3 GaAℓAs Heteroface Solar Cells

Late in the Phase 1 program detailed attention was given to the design of the GaAℓAs heteroface cell structures being prepared in the Task 4 effort, with particular attention to the parameters of the junction layer (i.e., the active p-type layer) of the $p^+Ga_{0.2}Aℓ_{0.8}As/pGa_{0.7}Aℓ_{0.3}As/nGa_{0.7}Aℓ_{0.3}As$ structures being grown by the LPE process. (See Section 2.5.1.)

There was concern at the time over the probable values of minority-carrier diffusion length that were being obtained in GaAℓAs heteroface cells made either by LPE or by MO-CVD techniques; for the MO-CVD case, at least, it had appeared that the L_n values were $\sim 0.5\mu m$, lengths significantly lower than those typical of GaAs. Because of the importance of designing cell junction depths to accommodate the carrier diffusion lengths characteristic of the material involved, an attempt was made to estimate the diffusion lengths being obtained in the LPE-grown alloy layers by matching the experimentally obtained spectral response data to a predicted response curve using the previously generated computer model for these cells along with various measured and/or estimated cell parameters.

This was done for an as-grown LPE cell the experimental photoresponse curve for which had been measured and corrected for illumination source spectrum and (approximately) for surface reflectivity based on previous measurements on other GaAlAs window layers. The result is shown in Figure 11 and indicates that a reasonably good match was obtained between modeled and measured (and corrected) data, for the set of cell parameters used with the computer model of the cell. These parameters are listed in Table 3.

It thus appears that minority carrier diffusion lengths in the n and p junction layers probably were in the 0.5-0.7μm range for this LPE cell, similar to the values that had been indicated indirectly for the MO-CVD alloy cells being grown at about the same time.

2.1.4 GaAs Window-type Solar Cells

This type of comparison of modeled and measured spectral photoresponse was next applied to GaAs window-type cells made by the molecular-beam epitaxy (MBE) process, as described in the Task 2 discussion (Section 2.2.2.3). The purpose again was to attempt to obtain a good match between measured (and corrected) spectral response curves for the GaAs cells and the response curves generated by the computer model based on certain cell parameters, and thereby to obtain an indication of the probable values of cell parameters such as minority carrier diffusion length in the junction layer. It was also intended that the response-matching process would provide guidance in the selection of certain cell design parameters, such as junction layer thickness, for experimental cell structures to be grown by CVD, MBE, or LPE processes. It was also planned that the modeling calculations be extended to two-cell SMBSC structures of GaAlAs-GaAs and of GaAs-Ge, but that work did not get started prior to the end of Phase 1. It will be undertaken in Phase 2, however.

When the analytical modeling procedure was applied to a high-quality GaAs heteroface cell made by MBE (see Figure 36 for typical illuminated I-V curve obtained with this structure) it was found that the various combinations of assumed parameters, when combined with known or measured parameters, did not produce an acceptable photoresponse match for the measured data (corrected for reflection losses) and at the same time yield a calculated J_{sc} value that was acceptably close to the value measured in the AM0 simulator.

Substantial effort was expended attempting to reconcile this discrepancy. The spectrometer was carefully checked and found not to be the cause of the problem. Attention was then turned to possible errors in the correction data used to account for reflection losses at the sample surface. A curve of reflectivity vs wavelength was calculated specifically for the cell in question, and it was found to differ by as much as 20 percent, at some wavelengths, from the reflectivity values which had been routinely used previously for correcting the photoresponse curves of GaAs heteroface cells. A major part of this discrepancy may have been caused by the fact that the window layer thickness on conventional heteroface cells of this type is usually the order of 1000Å while it was only ~400Å for the particular MBE cell of concern here. Use of the newly calculated reflectivity correction factors markedly improved the match between measured and modeled spectral response curves but was still not sufficient to produce an acceptable match between theory and experiment.

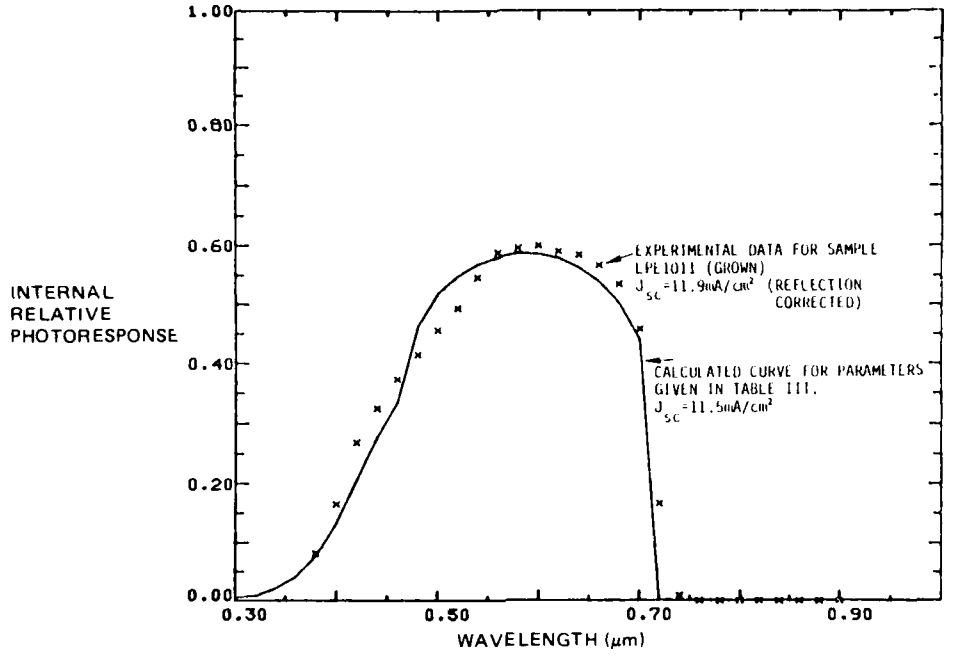


Figure 11. Measured and Calculated Photoresponse Data for As-grown GaAlAs Solar Cell of Sample LPE1011, Based on Corrected Experimental Photoresponse Curve and Computer Model Using Parameters of Table 3

Table 3. Parameters Used in Modeling Spectral Photoresponse of LPE-grown Solar Cell (Sample LPE1011).

Parameter	Value Used	Source/Basis for Value Used
Surface recombination velocity	10^6 cm/sec	Assumed
Window layer thickness	0.57μm	Measured on sample
Window layer Al content	x = 0.80	Nominal composition grown
Interfacial recombination velocity	10^3 cm/sec	Assumed
p layer thickness	0.71μm	Measured on sample
p layer Al content	x = 0.24	From measured photoresponse
n layer Al content	x = 0.24	Composition nominally grown to be same as p layer
n layer thickness	4.7μm	Measured on sample
Window layer diffusion length	0.1μm	Chosen for best fit
p layer diffusion length	0.7μm	Chosen for best fit
n layer diffusion length	0.5μm	Chosen for best fit
Mobility (all layers)	250 cm^2/V-sec	Assumed

Another attempt to improve the match was based on the argument that such a thin window might be only partially effective in mitigating the short-wavelength losses resulting from high surface recombination velocity. A sufficiently thin window could allow an excessive number of electrons to tunnel through the barrier and recombine at the GaAlAs/air interface. To model this possibility, a range of interface recombination velocities from 10^4 to 3 x 10^5 cm sec^{-1} was examined parametrically. Again it was not possible to obtain an acceptable match between measured and modeled spectral response while simultaneously satisfying the constraint imposed by the measured J_{sc}.

The problem had not been fully resolved by the end of the Phase 1 reporting period. It appears that the most likely cause of the problem, however, is inadequate data on the surface reflectivity of the specific cell involved. This would be remedied if specific reflectivity measurements were made for each cell examined.

2.2 GaAs-Ge SMBSC TECHNOLOGY DEVELOPMENT

The GaAs-Ge materials system is naturally lattice-matched, so a Ge-GaAs heterostructure tunnel junction could provide the solution to the problem of providing low-resistance current conduction across the interface of stacked GaAs and Ge cells. It would also be possible for this conducting tunnel junction to be entirely within the upper cell (GaAs) material.

This system also provides the opportunity for depositing the two cells on a relatively lower-cost material (viz, Ge) as well as one that is more robust and thus better able to resist process handling. One objective of this task was to determine which of the two possible substrate materials - Ge or GaAs - is more suitable for use in the two-cell SMBSC.

The program plan called for deposition of n^+GaAs on p^+Ge substrates and p^+Ge on n^+GaAs substrates to be undertaken first, to establish the growth conditions required for the conducting (nonrectifying) junctions in both cases. Emphasis was to be placed on determining deposition temperatures and subsequent heating cycles that would produce high interface doping concentrations and abrupt composition transitions. The dominant conduction mechanism was expected to be band-to-band tunneling, which would be investigated sufficiently to establish the conditions for obtaining the required low-resistance contact.

The growth of GaAs solar cell structures on Ge substrates was then to be undertaken, to establish the conditions for obtaining high-quality GaAs cell performance. Procedures and deposition conditions compatible with the requirements of the nonrectifying interfaces were to be emphasized and an optimum procedure sought.

Next, Ge solar cells were to be grown on Ge substrates, and conditions for obtaining high-efficiency Ge cell performance identified. Particular emphasis was to be placed on achieving high efficiency with surface doping concentrations compatible with the established requirements of the nonrectifying interfaces.

Following successful achievement of those specific tasks, the entire set of deposition procedures was to be integrated for the growth of the two-cell (GaAs and Ge) SMBSC structure on Ge substrates. The required cell fabrication procedures were to be developed, and the resulting two-cell assembly then characterized (Task 6) and its properties carefully assessed.

It was intended that Ge p-n junction cells would also be grown in an inverted configuration on GaAs substrates, with the resulting structure $nGe/p^+Ge/n^+GaAs$. Photovoltaic characterization of such a structure would be accomplished by obtaining front access to the p^+Ge layer by selective etching or by contacting it through the n^+GaAs. Layer thicknesses and doping concentrations were to be chosen for best photovoltaic device performance, after which comparison with the performance of Ge junction cells on Ge substrates would be made.

Following successful fabrication of these Ge cells on GaAs (assuming the required growth conditions for the nonrectifying interfaces were by that time established, as discussed above), the two-cell (GaAs and Ge) SMBSC assembly would

then be grown on GaAs substrates. This would be accomplished by growing the Ge cell on the back (n^+) side of GaAs solar cell structures consisting of MO-CVD layers on GaAs n^+ substrates. The photovoltaic properties of the two-cell SMBSC's would then be determined.

Based on the results of such measurements and on similar results obtained for the two-cell GaAs-Ge SMBSC structures prepared on Ge substrates, one of the configurations, both of which are shown schematically in Figure 12, was to be selected for further optimization in order to maximize the overall efficiency of the GaAs-Ge two-cell assembly.

In the original program plan the GaAlAs/GaAs cell structures to be used in this task were all to be grown by the MO-CVD process and the Ge layers required for the Ge cells were to be grown by a conventional CVD reaction, such as GeH_4 pyrolysis or $GeCl_4$ reduction – the choice to be made after further consideration of the detailed requirements of the layers. Late in the Phase 1 program, however, as indicated earlier, a change in program emphasis allowed the option of supplementing the CVD techniques with other processes when doing so appeared to improve the prospects of achieving the overall program goals. Thus, the MBE growth of both GaAs and Ge cell structures became incorporated into the activities of this task.

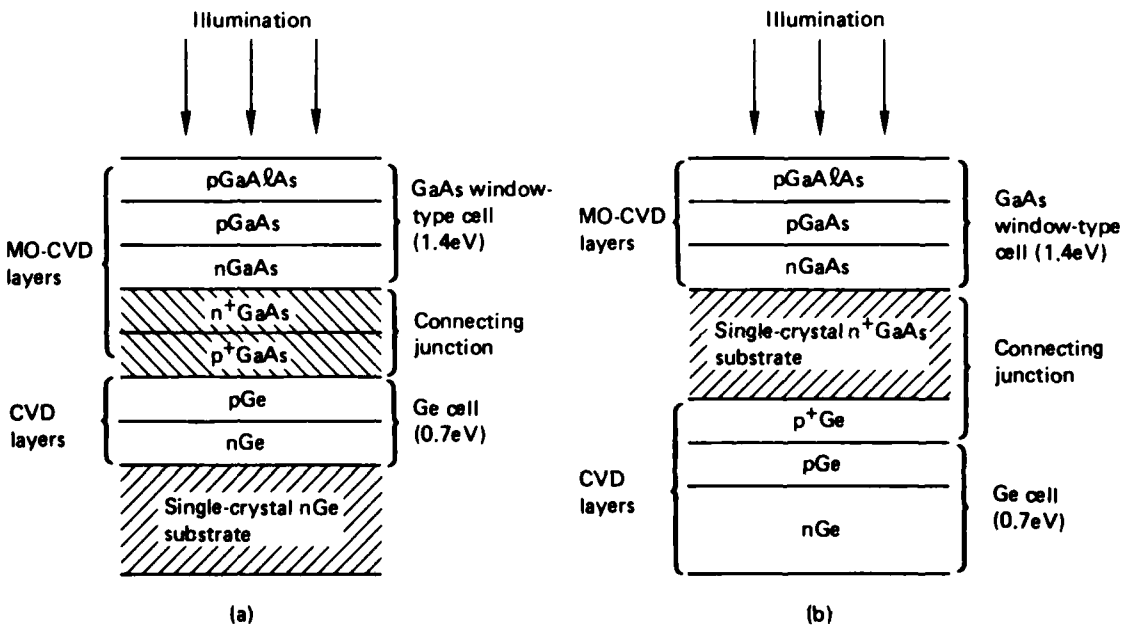


Figure 12. Two Possible Configurations of GaAs-Ge Two-cell SMBSC Assembly. a) Structure Using Ge Single-crystal Wafer as Base; b) Structure Built on GaAs Single-crystal Wafer

This section contains descriptions of the preparation and characterization of GaAs solar cells made by MO-CVD and by MBE techniques; the preparation and characterization of Ge solar cells made by CVD, MBE, and thermal diffusion techniques; the preparation and evaluation of connecting intercell junction structures made by MO-CVD and MBE methods; and the fabrication of experimental GaAs-Ge SMBSC structures.

2.2.1 Properties of GaAs-Ge Interface

Of the two possible configurations to be investigated for this two-cell SMBSC – one on a GaAs substrate and one on a Ge substrate – the most desirable one is that involving the Ge substrate. In that configuration a GaAs cell is grown on a Ge cell on the Ge substrate, thus utilizing the larger-area less brittle Ge wafers and allowing higher overall yields in the device fabrication process.

A major requirement for successful use of this configuration is growth of an abrupt and structurally perfect interface between the GaAs and the Ge, especially if the connecting junction between the two cells is to be a tunneling heterojunction. A series of samples consisting of thin (~400Å) layers of GaAs on (100)-oriented single-crystal Ge substrates was grown by MO-CVD. The composition of these films near the interface was analyzed by Auger electron spectroscopy combined with simultaneous etching of the sample surface by argon ion sputtering. The apparent widths of the GaAs-Ge heterostructure transition regions, as determined by the spatial distribution of the principal chemical species involved (viz, Ga, As, and Ge, as well as oxygen), were found to be dependent upon the particular growth conditions employed during the initiation of the GaAs layer growth on the Ge substrate surface. The minimum "interface width" of ~45Å was determined to occur for films prepared with the TMGa and the arsine (AsH_3) introduced simultaneously into the deposition chamber to start the GaAs layer growth.

Those growth conditions were then used to deposit GaAs p-n junction structures and complete GaAlAs-GaAs heteroface solar cell structures on n-type (0.001-0.040 ohm-cm) Ge single-crystal substrates, described in Section 2.2.2 below.

Although some experimental n^+ GaAs/p^+Ge heterostructures were grown early in the program for preliminary evaluation, attention shifted at an early date to n^+/p^+ as well as p^+/n^+ structures grown entirely in GaAs layers on both GaAs and Ge single-crystal substrates, for possible use as the conducting tunnel junction between cells in the GaAs-Ge SMBSC. Such n^+GaAs/p^+GaAs structures were also used in some of the first GaAlAs-GaAs two-cell SMBSC's, as described in Sections 2.4.2 and 2.4.3. The preparation and properties of these GaAs n^+/p^+ and p^+n^+ structures are discussed in Section 2.2.4.

2.2.2 GaAs Solar Cells for GaAs-Ge SMBSC's

The MO-CVD parameters found to produce the most abrupt transition from the Ge substrate to the deposited GaAs film in the heterostructure samples described in Section 2.2.1 were used to prepare GaAs p-n junction structures on n-type Ge (100)-oriented substrates as well as complete GaAs heteroface solar cell structures (with

~800Å window layers of $Ga_{0.2}Al_{0.8}As$) on similar substrates. Typical active layer thicknesses were 1.0-1.5 μm for the Zn-doped p-type layer and 3-5 μm for the Se-doped n-type layer. A number of deposition experiments were also carried out at this same time, early in the program, to confirm the reproducibility of the p- and n-type GaAs doping conditions to be used in preparing p-n junction, tunnel junction, and alloy window-layer structures.

Some difficulties were encountered, however, when the above junction and cell structures were being processed into completed devices. During the contact definition step the contact patterns repeatedly lifted off, for reasons not then known. Some of the relatively large-area (2 cm x 2 cm) GaAlAs-GaAs heteroface cell structures were set aside for use in trouble-shooting the contact lift-off procedure and contact metallization process. Other samples in the group were processed into small (50 mil x 50 mil) mesa-type devices to avoid the contact definition problem and allow evaluation of the device structures.

The investigation of the GaAs cell contact definition and metallization procedure, the preparation and properties of MO-CVD GaAs cells, and the preparation and properties of MBE GaAs cells are discussed in the next three subsections.

2.2.2.1 Contact Definition and Metallization

Several of the large-area GaAlAs-GaAs heteroface cell structures prepared early in the program were used for tests of the vacuum-deposited Ag-Mn composite being used for the p-type contact. A general improvement of the contact deposition and alloying procedure and further work with the lift-off technique used for contact definition, involving the use of thicker photoresist layers and thinner Ag-Mn metallization layers, resulted in better contact pattern definition. It was also found necessary to deposit a thin overlay of Au on the Ag-Mn contact to reduce tarnishing. This was done routinely thereafter.

In the fifth month of the program a new experimental cell processing mask set, designed earlier in the program, was received and put into use immediately. This mask set made it possible to process an array of 0.5 cm x 0.5 cm individual devices on each multilayer sample. The sample could then be characterized as a single wafer or as a group of separate cells after sawing into individual 0.5 cm x 0.5 cm devices using a Tempress Model 602 Dicing Saw with suitable microthin blade.

Figure 13 shows a macrophotograph of a typical array of 0.5 cm x 0.5 cm GaAlAs-GaAs cells grown by MO-CVD and processed with this mask set on a single-crystal GaAs substrate of approximate dimensions 3.7 cm x 2.1 cm.

As the 0.5 cm x 0.5 cm cell size came to be used as the standard for evaluation of the various cell structures grown by CVD methods it was also noted that significantly different I-V curves could be obtained for a given cell by varying the illumination conditions in the customary test arrangement being used for rapid screening of cell properties. This simplified experimental arrangement involved a tungsten-filament microscope lamp, the illumination from which was incident normally on the cell surface from a distance that was adjusted so that the short-circuit current of the cell was ~10mA. This "standardized" arrangement permitted

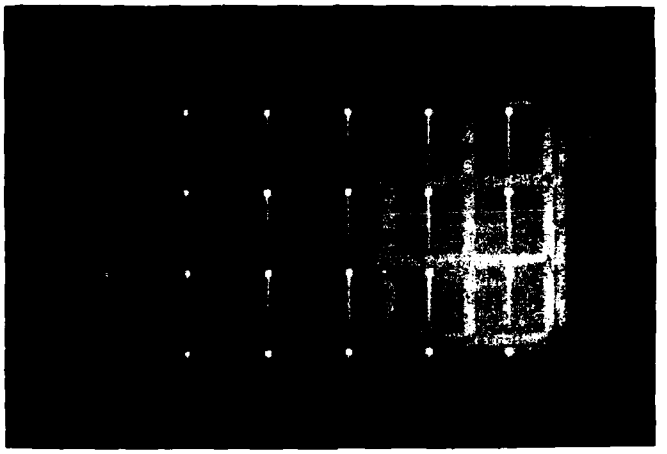


Figure 13. Photograph of Typical Array of 0.5 cm x 0.5 cm GaAlAs-GaAs Cells Grown by MO-CVD and Fabricated on Single-crystal GaAs Substrate ~3.7 cm x 2.1 cm

rapid evaluation of cell performance under illumination that was infrared-rich and of somewhat greater total intensity than AM0 (135 mw/cm^2), but which nonetheless permitted valid comparisons of relative cell performance.

However, because of the nonuniform intensity across the cross-section of the illuminating beam and the relative dimensions of the cells and the beam at the cell surface, it was possible to obtain different cell responses by shifting the center of the beam across the sample surface. Thus, when the region of illumination was centered near the probe contact the I-V curve exhibited a better fill factor (for the 10mA short-circuit current) than that obtained for the same short-circuit current value with the illumination centered at the opposite end of the cell. This effect is illustrated in Figure 14, which shows I-V curves for one of the 0.25cm^2 cells illuminated (a) close to the probe contact pad and (b) at the end of the cell opposite the contact pad.

This effect was believed to be caused by the series resistance of the metal contact pattern and/or by the resistance of the metal-semiconductor contact interface. A brief investigation of contact metallizations of differing dimensions indicated that the metal contacts would have to be "up-plated" to increase the cross-sectional area of the conducting paths and thus reduce the series resistance of the contact pattern in subsequent refinements of the 0.5 cm x 0.5 cm experimental cell design. There was no indication that the specific contact resistance was a limiting factor.

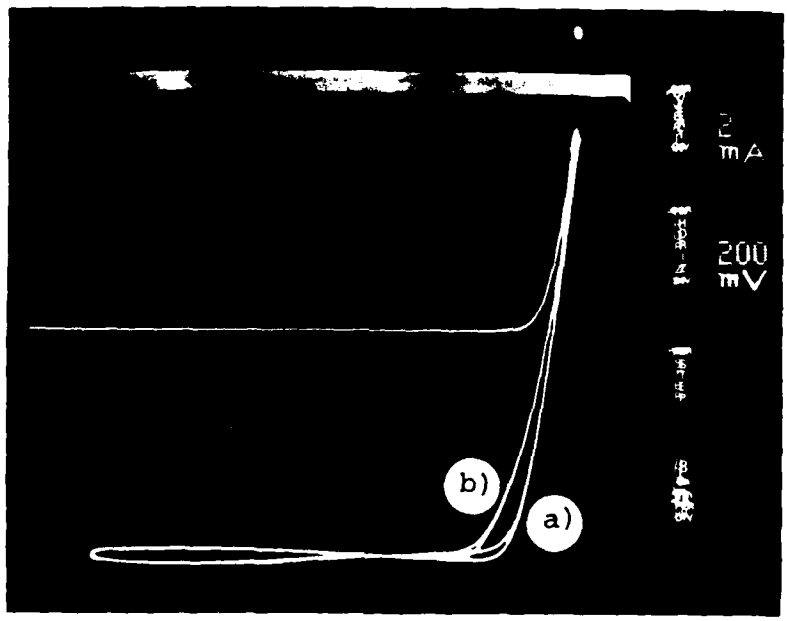


Figure 14. Illuminated (microscope lamp) I-V Characteristics of Conventional GaAlAs-GaAs Thin-window Heteroface Solar Cell Structure Grown by MO-CVD at 750°C on GaAs Single-crystal Substrate, Showing Effect on Fill Factor of Centering Illumination (a) Near Metal Contact Pad at Edge of 0.5cm x 0.5cm Cell, and (b) Near Opposite Edge of Cell

2.2.2.2 GaAs Cells Made by MO-CVD

Most of the GaAs heteroface cells prepared during Phase 1 were grown on GaAs single-crystal substrates; many cells, however, were also prepared on Ge single-crystal substrates. Of the GaAs cells grown on GaAs substrates, by far the greatest number were grown by the MO-CVD process, although in the final three months of Phase 1 a number of such structures were prepared by MBE, as indicated earlier.

The work with GaAs cells formed by the MO-CVD process on both GaAs and Ge substrates is reviewed in the next two subsections.

2.2.2.2.1 MO-CVD GaAs Cells on GaAs Substrates. High efficiency GaAs heteroface solar-cells (η= 12.8 percent, AM0, no AR coating) had been previously prepared at Rockwell by the MO-CVD technique on single-crystal GaAs substrates (Ref 8), but it was necessary to verify all aspects of that previously established capability for application to this program.

Early in the program some exploratory [illegible] GaAs p-n junction cell structures, with no GaAlAs window layer, were grown by MO-CVD on GaAs substrates. Active layer thicknesses similar to those used for conventional window-type GaAlAs-GaAs solar cells were used. The I-V characteristics of those structures looked quite good, with no evidence of either excess leakage or excess series resistance.

These reassuring but preliminary results provided the impetus for a series of deposition experiments in which GaAs heteroface cell structures (with windows) were deposited simultaneously on n-type (100) GaAs and n-type (100) Ge substrates. These experiments are discussed further in Section 2.2.2.2.2, but in general the properties of the GaAs cells that resulted were considerably poorer than those of earlier GaAs heteroface cells prepared on GaAs substrates by MO-CVD at Rockwell.

An indication of the performance obtained with GaAs heteroface cells prepared in structures grown separately on GaAs substrates during the first several months of the program is seen in Figure 15. This shows the dark and illuminated (microscope lamp) I-V characteristics of a 0.5cm x 0.5cm GaAlAs-GaAs window-type solar cell processed in a *multilayer* sample grown on a (100) GaAs:Si substrate. A relatively low fill factor of about 0.68 is observed, with a V_{OC} value of ~0.97V and a short-circuit current density of ~20mA cm^{-2} for the tungsten-lamp illumination involved.

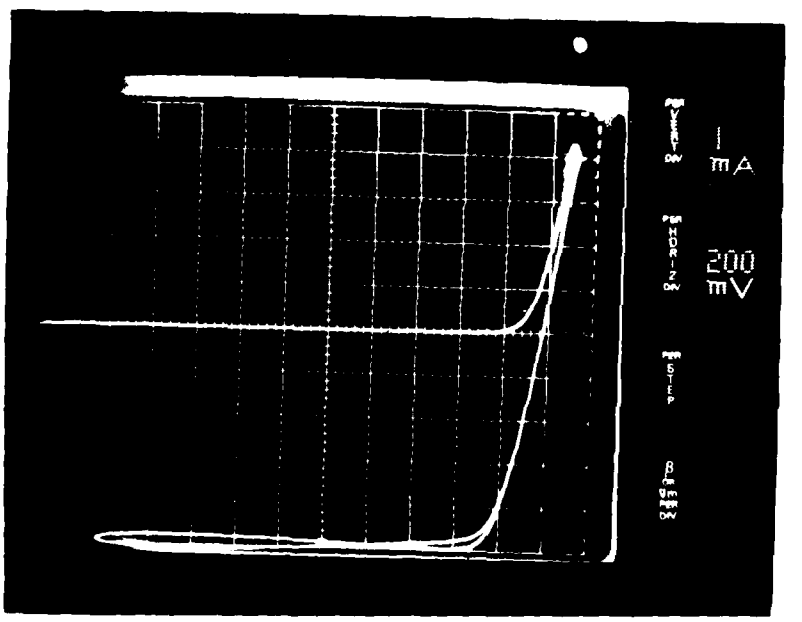


Figure 15. Dark and Illuminated (microscope lamp source) I-V Characteristics of GaAlAs-GaAs Window-type Solar Cell Grown by MO-CVD on Single-crystal GaAs:Si Substrate Early in Phase I Program (Cell area 0.5cm x 0.5cm)

By the midpoint of the Phase 1 program the results had improved considerably, but the efficiencies being obtained with GaAlAs-GaAs heterolace cells made by the MO-CVD process were still lower than expected. Most of the cell structures had been grown at 700°C, but experiments were begun to establish the proper deposition parameters for MO-CVD growth of doped and undoped GaAs and GaAlAs layers at 700°C and 650°C. Growth of several undoped GaAs films on GaAs:Cr substrates established (by transport measurements) that the background (n-type) doping level in the reactor system was then $\sim 1 \times 10^{14} cm^{-3}$ for deposition at 700°C with a H_2 flow rate of 7.0 ccpm through the TMG source and an AsH_3 (10 percent in H_2) flow rate of 150 ccpm.

The photoresponses of some of the cells prepared during this period were measured using both microscope lamp illumination and simulated (but not spectrally matched) AM0 illumination from a xenon arc lamp. A typical set of dark and illuminated I-V curves for one of these devices is shown in Figure 16, in this case for illumination with the microscope lamp. The cell structure represented was deposited at 750°C on a (100) GaAs:Si substrate. The V_{oc} value for this cell is seen to be about 0.94V and the J_{sc} value approximately 38mA cm^{-2} for the infrared-rich high-intensity illumination of the microscope lamp. When this and other cells on this same substrate were measured in the AM0 simulator the typical parameters were V_{oc} 0.91V, J_{sc} 17.3mA cm^{-2}, FF 0.78, and η 9.1 percent, with no AR coating and without correction for area loss due to contact coverage.

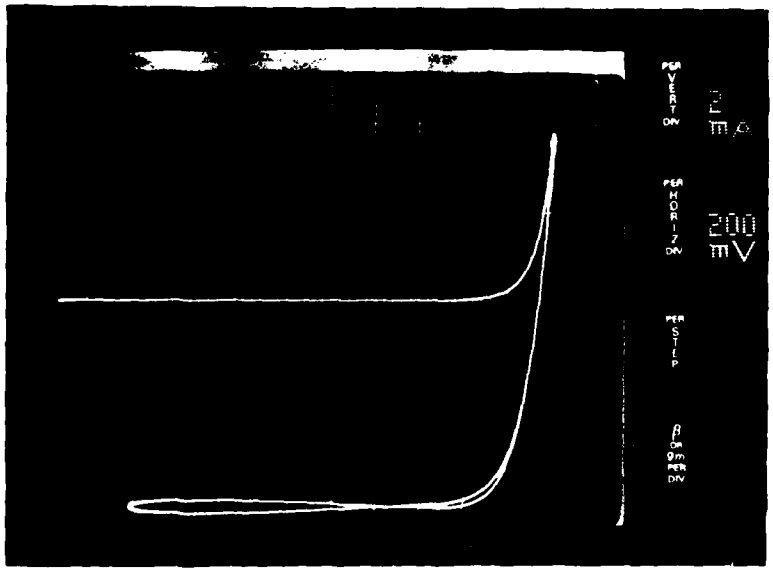


Figure 16. Dark and Illuminated (microscope lamp) I-V Characteristics of 0.5cm x 0.5cm GaAlAs-GaAs Window-type Solar Cell Deposited by MO-CVD at ~750°C on (100) GaAs:Si Substrate Midway through Phase 1 Program

The cause of the lower-than-expected efficiencies in the GaAlAs-GaAs heteroface cells being grown by MO-CVD was not known. A systematic examination of the problem was undertaken, with particular attention given to the details of processing the multilayer cell structures into individual finished devices and to the question of possible unexpected (and unidentified) impurities entering the structures during the MO-CVD growth process, presumably from one of the reactant source tanks. Although no obvious problems in either film growth or device processing were found in this investigation, continued improvement in results was noted soon thereafter.

GaAs heteroface cell structures grown separately on (100)GaAs:Si substrates in the following month were processed as usual into arrays of individual 0.5cm x 0.5cm cells which were then tested by measurement of dark and illuminated I-V characteristics using mechanical probe contacts, the microscope lamp, and a curve tracer. Further evaluation of the best devices on some of the wafers was then accomplished by mounting and bonding individual cells to TO-16 headers and measuring the I-V curves under simulated AM0 illumination with the xenon lamp.

Results typical of those GaAlAs-GaAs cells grown separately on the (100)GaAs:Si substrates are shown in Figures 17 and 18. Figure 17 shows the dark and illuminated I-V characteristics of an uncoated cell tested with the microscope lamp and probe contacts. As a convenience in rapidly screening these devices with this simplified procedure the intensity of the incident illumination was adjusted by changing the lamp-to-cell distance. The intensity was usually so adjusted to produce a ~10mA short-circuit current, as noted earlier. The cell quality could then be estimated readily by examination of the curve shape (i.e., fill factor) and the open-circuit photovoltage V_{OC}.

Figure 18 shows the I-V curves for another uncoated cell fabricated on the same GaAs substrate wafer but after its mounting and bonding on the header, with the AM0 simulator as illumination source. This cell is seen to exhibit a good V_{OC} value (0.97V) and a fairly good fill factor (0.78), but the short-circuit current density is again only about 17.0 mA/cm^2. The efficiency is thus ~9.6 percent.

The heteroface GaAs cells grown on GaAs substrates in the next series of devices showed additional improvement. Some of these cells were grown at ~700°C and some at ~750°C. The wafers were processed into the usual 0.5cm x 0.5cm cells and tested with the microscope lamp illumination; individual cells were tested in this way, using mechanical probe contacts, prior to sawing the wafer into separate cells for mounting on TO-16 headers. It was thus easy to construct a "map" of the photovoltaic response over the entire wafer, and this procedure showed generally a high degree of uniformity of photovoltaic properties except where there were obvious substrate defects. Such defects were readily identified in the GaAs substrates after the polishing process (done at Rockwell), and most often appeared to be in regions where the GaAs crystal growth in the original boule had become locally polycrystalline.

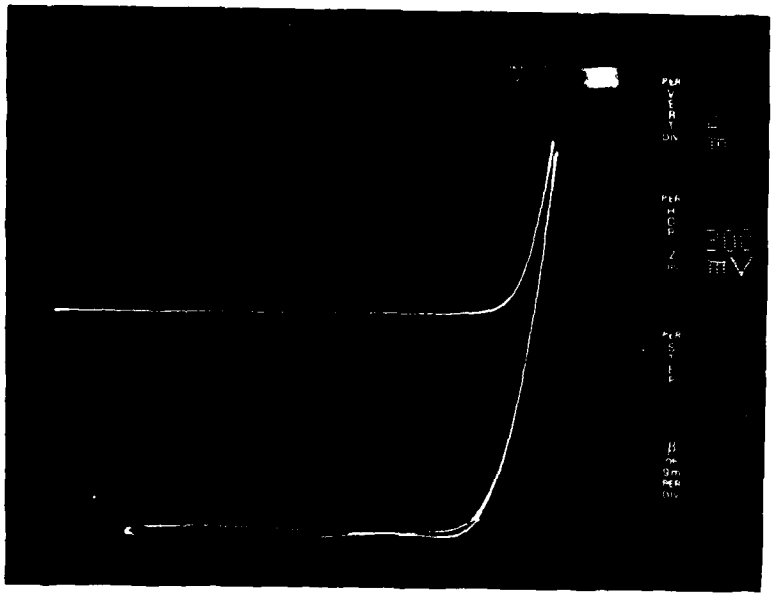


Figure 17. Dark and Illuminated (microscope lamp) I-V Characteristics of GaAlAs-GaAs Thin-window Heteroface Solar Cell Grown by MO-CVD at 750°C on (100)GaAs:Si Substrate (No AR coating on cell)

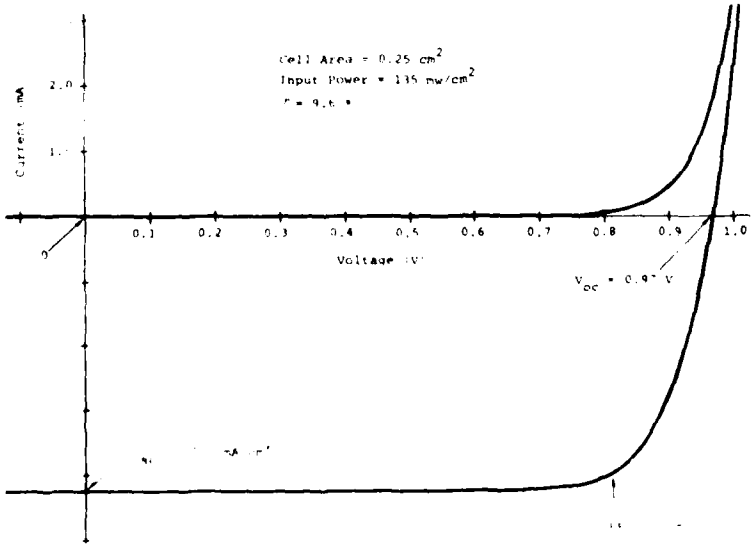


Figure 18. Dark and Illuminated (xenon lamp AM0 simulator, 135 mw/cm²) I-V Characteristics of GaAlAs-GaAs Thin-window Heteroface Solar Cell Grown by MO-CVD at 750°C on Same (100)GaAs:Si Substrate as Cell of Figure 17 (No AR coating on cell)

Typical I-V characteristics (dark and illuminated by the microscope lamp) for the better cells in samples grown at ~700°C and ~750°C are shown in Figures 19 and 20, respectively. Comparison of these results with those of Figures 16 and 17 shows that the later cells were generally improved over those previously prepared. The later cells all involved Te-doped n-type GaAs substrates, while most of the earlier cells described were on Si-doped GaAs substrates. It did not necessarily appear, however, that the improvement in cell performance was related to the change to Te-doped substrates, especially since the latter have been found typically to have a high incidence of structural imperfections.

Also grown at about the same time were several conventional GaAlAs-GaAs heteroface solar cell structures having somewhat thinner p-type GaAs:Zn layers and thinner $Ga_{0.2}Al_{0.8}As$:Zn window layers than those normally grown. The p-type active layers in these cells were ~0.75 μm thick instead of the usual 1.0 μm, and the window layers were ~500Å instead of the ~1000Å most often used in these cells. It would be expected that improved short-circuit current and better AM0 spectral response would result for these modified cells. The dark and illuminated I-V characteristics for one of the 0.5cm x 0.5cm cells fabricated in one of these structures are shown in Figure 21, for illumination with the microscope lamp. It appears that somewhat improved photovoltaic response was indeed achieved by the modifications in cell design.

As part of the investigation of possible causes of the lower-than-expected AM0 efficiencies being obtained in the GaAs heteroface cells prepared by MO-CVD, a number of the 0.5cm x 0.5cm GaAs window-type cells were characterized with the calibrated Spectrolab Model XT-10 simulator (AM0, xenon source) at the Rockwell Satellite Systems Division at Seal Beach, CA. The simulator used earlier at Rockwell ERC involved an unfiltered 1000-watt xenon lamp, and this source is known to have a spectral output that is not a very good match to the AM0 spectrum. This raised the obvious question of the effect upon measured cell performance of departures of the simulated AM0 spectrum from the proper AM0 spectrum, although for most non-critical measurements the unfiltered lamp provided an acceptable measure of "AM0 response."

The group of cells measured in the Seal Beach simulator involved four different substrate wafers and had not been previously evaluated with the ERC simulator. The simulator output was set for 129 mw/cm^2 by means of a calibrated Si reference cell. For this AM0 simulated insolation the cells measured had efficiencies of up to 11.5 percent, with no AR coating. If a multiplying factor of 0.95/0.66 = 1.44 is applied to correct for the anticipated effect of a good AR coating it follows that the above maximum corresponds to an efficiency of 16.6 percent with coating. Although this is still not as high as the previous best performance achieved with such a cell made at Rockwell by MO-CVD, the result did provide an adequate baseline reference for comparison of the various SMBSC's under development in this program. Figure 22 shows the fourth-quadrant I-V curve for the 11.5 percent cell under AM0 illumination of 129 mw/cm^2, as obtained in the above measurements.

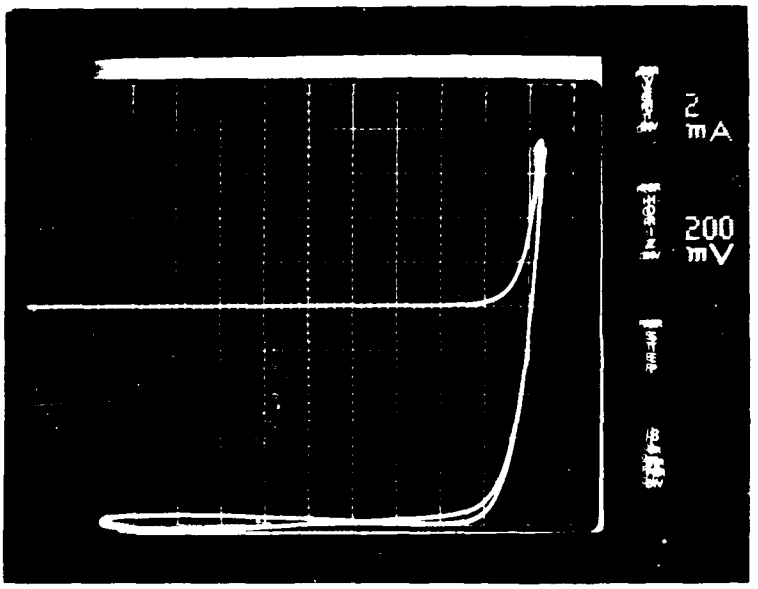


Figure 19. Dark and Illuminated (microscope lamp) I-V Characteristics of Conventional Thin-window GaAlAs-GaAs Heterojace Cell (0.5cm x 0.5cm) Grown by MO-CVD at ~700°C on Single-crystal GaAs:Te Substrate

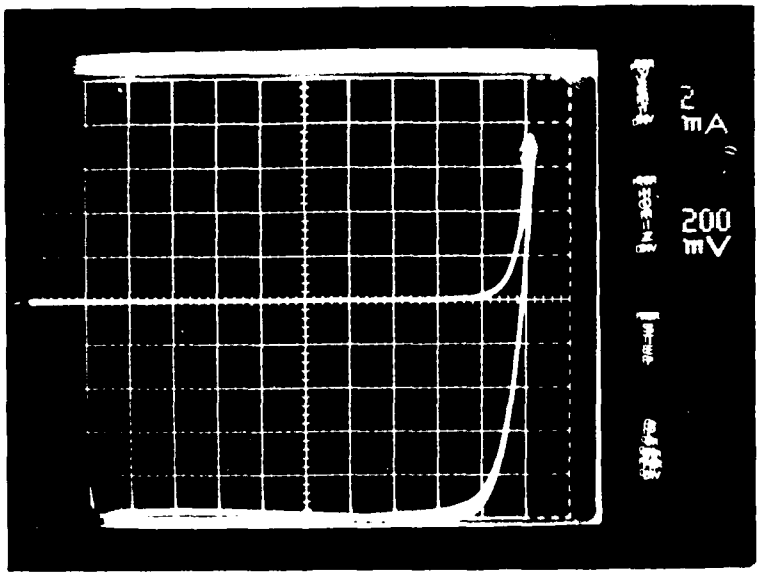


Figure 20. Dark and Illuminated (microscope lamp) I-V Characteristics of Conventional Thin-window GaAlAs-GaAs Heterojace cell (0.5cm x 0.5cm) Grown by MO-CVD at ~700°C on Single-crystal GaAs:Te Substrate

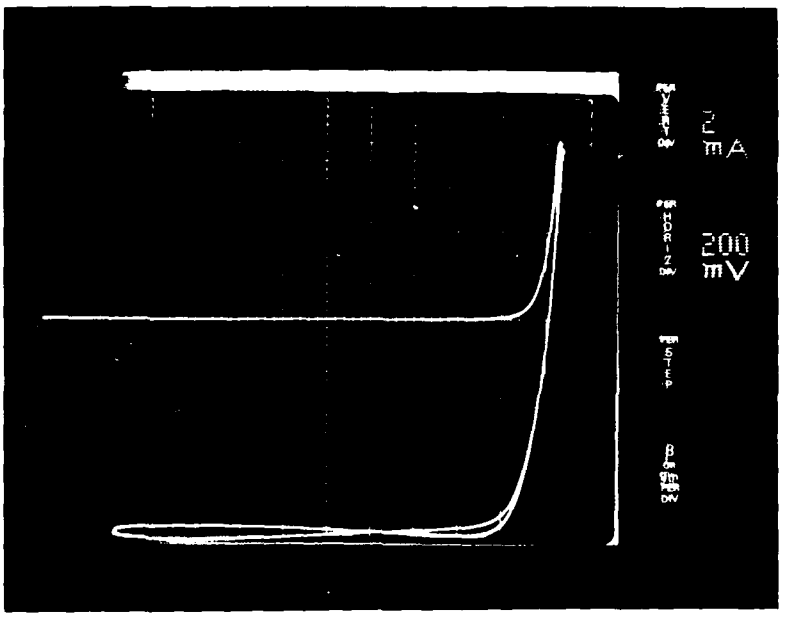


Figure 21. Dark and Illuminated (microscope lamp) I-V Characteristics of Thin-window GaAℓAs-GaAs Heteroface Solar Cell (0.5cm x 0.5cm) Grown by MO-CVD at ~750°C on Single-crystal GaAs:Te Substrate; Both Window Layer and p-type Active Layer Thinner than Usual (see text)

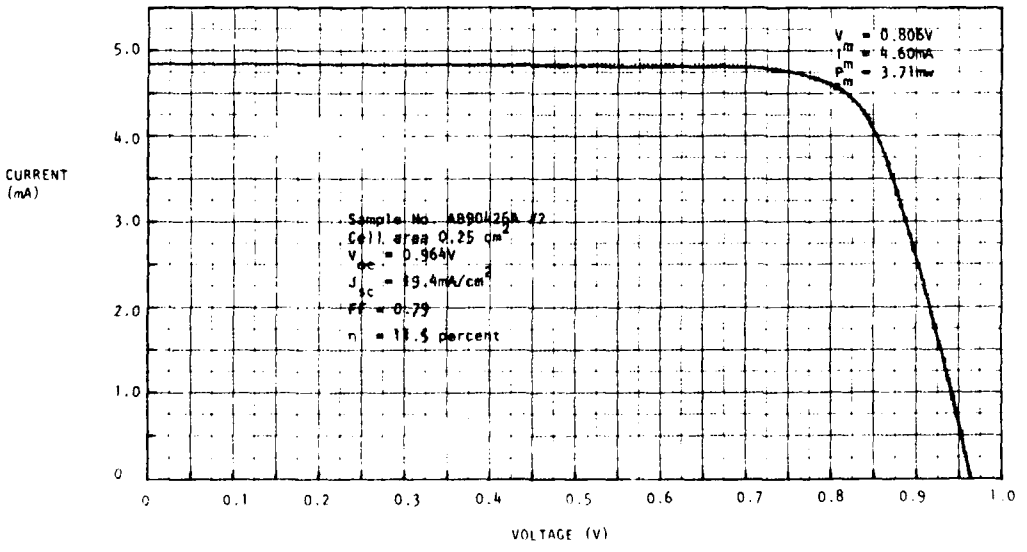


Figure 22. Fourth-quadrant I-V Characteristic of GaAℓAs-GaAs Window-type Heteroface Solar Cell (0.5cm x 0.5cm) Made by MO-CVD, under Simulated AM0 Illumination of 129 mw/cm^2 from Calibrated Simulator

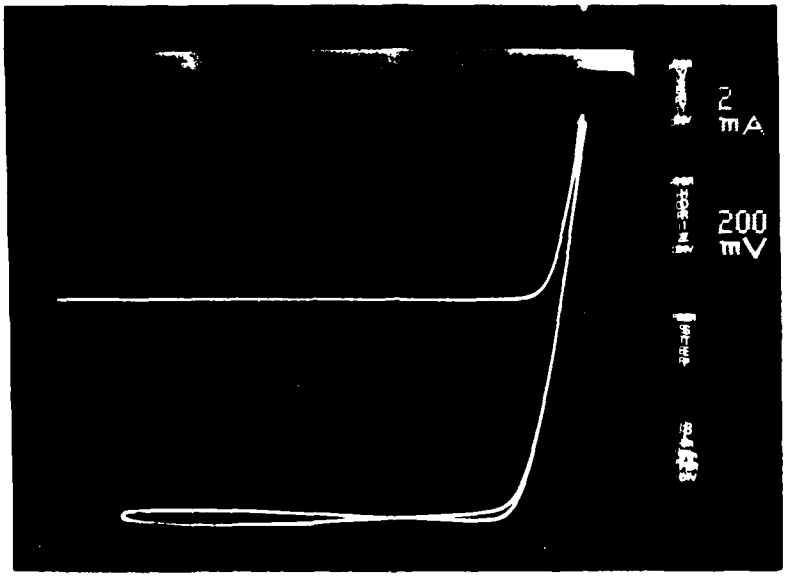
Shortly after the above cell structures were grown it was noted, by careful SEM and optical microscope examination, that the layer thicknesses in various single-cell and two-cell SMBSC structures were much less than was expected on the basis of the deposition parameters used. The apparent cause of this was that a new mass-flow controller had been installed in the TMG source line of the reactor system just prior to the growth of these structures, because of functional problems that had developed with the controller previously in use. The new unit, however, had evidently been miscalibrated at the factory (Tylan Corp., Torrance, CA) so that thicknesses of layers involving Ga as a constituent turned out to be quite different from expected values.

After this problem was corrected and the necessary growth parameters had been reestablished, a number of conventional GaAlAs-GaAs thin-window heteroface solar cell structures on GaAs substrates were prepared by deposition at 750°C. The structure (i.e., layer thicknesses and doping concentrations) of these composites was varied slightly to determine the effect of such parameter variations on the performance of the resulting cells. As customary, the wafers were processed into arrays of 0.5cm x 0.5cm (0.25 cm^2 area) individual cells. The resulting cells were evaluated using the microscope lamp and mechanical probes.

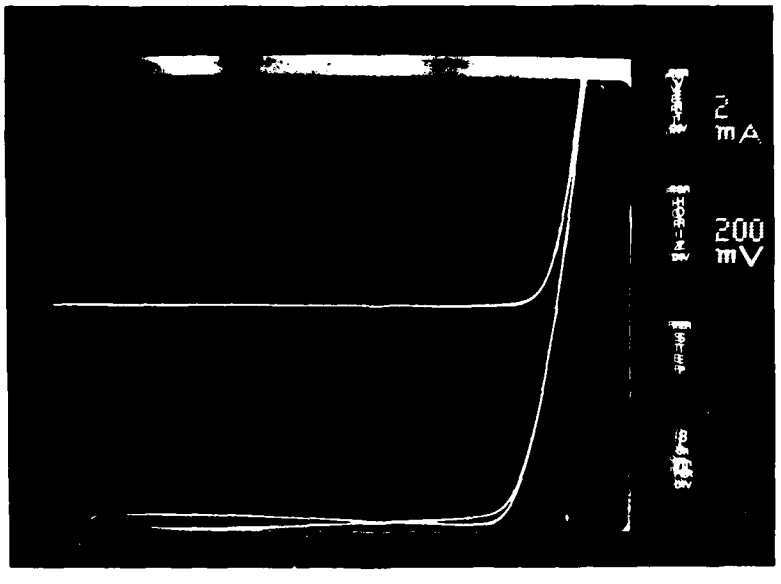
Typical I-V characteristics obtained for cells on some of the best wafers are shown in Figure 23. As in previous cell characterization using the microscope lamp the intensity was set to produce a short-circuit current of 10mA for the cell under test. It can be seen that V_{oc} values of 1.0V were obtained, with good curve shapes (fill factors).

Spectral response measurements were made on some of these GaAs cells using the grating spectrometer and detector system at ERC Anaheim. This equipment uses a 100-150 watt tungsten-halogen lamp in conjunction with a Spex 1.4-meter grating spectrometer and appropriate focusing optics. The throughput of the system operating at 100Å resolution generates a short-circuit current density in a cell that is approximately $10^{-3} \times J_{sc(AM0)}$. For accurate quantitative spectral response data the cells should be AR-coated, but accurate comparisons of individual cells on a given substrate wafer can be made without the coating. Data for photoresponse as a function of wavelength for both a reference cell and the experimental cell and quantum efficiency data for the reference cell are put into digital form and manipulated by a Hewlett-Packard 9825A computer. The output is the response of the experimental cell as a function of wavelength normalized for unit input intensity.

Figure 24 shows data for two conventional GaAlAs-GaAs thin-window heteroface solar cells (0.5cm x 0.5cm) grown by MO-CVD at 750°C on a GaAs substrate (i.e., both cells are on a common substrate). One of the two cells is the cell the I-V curves for which are shown in Figure 23a. Coincidence of the point-by-point spectral response data for the two cells is striking and attests to the uniformity of results obtained by the MO-CVD process over the area of a typical 2cm x 4 cm substrate. The sharp drop in response at long wavelengths corresponds to the expected behavior at the bandgap energy of GaAs. Both cells maintain essentially maximum response for higher-energy illumination throughout the visible region, still exhibiting >80 percent of maximum response at wavelengths as short as ~0.475 μm.



(a)



(b)

Figure 23. Dark and Illuminated (microscope lamp) I-V Curves of Two Conventional GaAlAs-GaAs Thin-window Heteroface Solar Cells (0.5cm x 0.5cm) Grown by MO-CVD at 750°C on Different Single-crystal GaAs Substrates after Recalibration of Mass Flow Controller

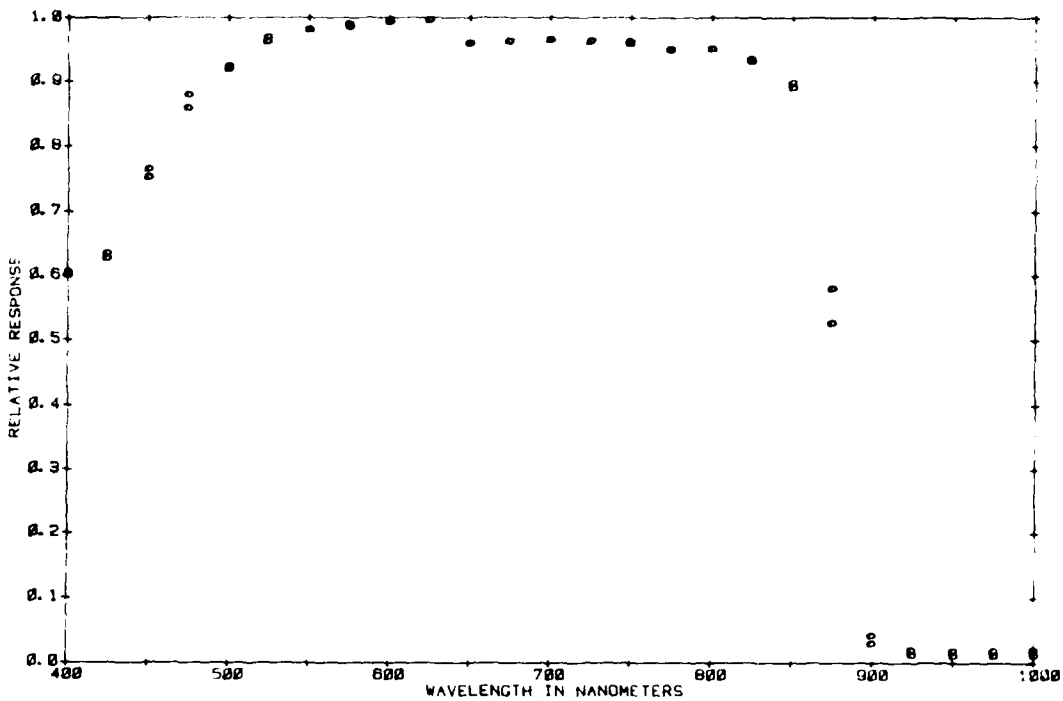


Figure 24. Spectral Response Data for Two Different GaAlAs-GaAs Heteroface Solar Cells (0.5cm x 0.5cm) Processed in MO-CVD Layers Grown at 750°C on One GaAs Substrate Wafer

Thus, although the previous high-efficiency cell performance was not successfully duplicated by the GaAs heteroface cell structures made by MO-CVD during the Phase 1 program, cells having acceptable AM0 performance were being fabricated by the end of the period covered by this report. It did not appear that variation in deposition temperature in the 700-750°C range produced significant differences in cell performance, but thinner window layers (~500Å) and thinner p layers (~0.75μm) in the active GaAs region did appear to produce improved photovoltaic response. The performance obtained with the GaAs cell structures prepared in the later stages of Phase 1 was judged to be sufficiently good to allow program attention to be concentrated on developing the GaAlAs cell and the Ge cell, both intended for use in conjunction with GaAs cells in SMBSC configurations.

Also, and perhaps more importantly, the capability for growing GaAs heteroface cell structures with overall dimensions of 2cm x 4cm or more (see Figure 13) and with a high degree of uniformity of properties over similar large areas (see Figure 24) had been clearly demonstrated. This constitutes a major step toward achievement of the contract goals.

2.2.2.2.2 MO-CVD GaAs Cells on Ge Substrates. Since the preferred two-cell GaAs-Ge SMBSC configuration, from the standpoint of materials cost and device durability, is that in which the Ge and GaAs cells are deposited in sequence on a Ge single-crystal substrate (see Figure 12a), it was considered important to develop

the capability for obtaining high quality GaAs cell structures on Ge by one or more of the deposition techniques being used. Consequently, the first GaAs cell structures prepared in this program were grown by the MO-CVD process on Ge substrates, as pointed out previously.

The GaAs MO-CVD growth parameters that had produced the most abrupt transition from Ge to GaAs at the growth interface in samples that had been analyzed by Auger electron spectroscopy (see Section 2.2.1) were used to prepare GaAs p-n junction device structures on low-resistivity (0.001-0.040 ohm-cm) n-type (100)-oriented Ge single-crystal wafers. Typical n layer thicknesses were 3-5 μm and p layer thicknesses were 1.0-1.5 μm. Some of the structures also had $Ga_{0.2}Al_{0.8}As$ window layers $\leq$0.1 μm thick. Problems were encountered in processing these first structures into completed large-area cells, as noted earlier, due to contact adherence and lift-off difficulties.

To circumvent the large-area contact problem temporarily a number of small (50 mil x 50 mil) mesa-type devices were fabricated in these structures, some of which were grown at ~700°C and some at ~750°C. Those grown at 750°C were found to be considerably more leaky than those grown at the lower temperature, suggesting at first that MO-CVD growth of GaAs on Ge might best be done at lower-than-customary temperatures to avoid defect formation at the growth interface. Those devices grown at ~700°C exhibited good forward and reverse I-V characteristics.

Some large-area (2cm x 2cm) cells grown on Ge substrates at ~750°C were successfully processed, including some with and some without GaAlAs window layers. Although the structures grown on GaAs substrates at about the same time showed relatively good I-V characteristics (neither excess leakage nor excess series resistance), those grown on Ge substrates exhibited the same leaky I-V characteristics as were seen for the small mesa devices mentioned above. The fill factors were poor, so the efficiencies were very low.

Shortly thereafter, another group of GaAs p-n junction structures and GaAs heteroface solar cell structures was grown on (100)GaAs and (100)Ge n-type single-crystal substrates. The structures on Ge were deposited at 700 and 750°C, as were those in the previous group. Small-area (50 mil x 50 mil) mesa devices with 25 mil x 25 mil contact pads were again fabricated. As for the earlier group of similar devices, those grown at 700°C had somewhat better (less leaky) I-V curves than did those grown at 750°C.

One of the GaAs p-n junction structures was grown on a Ge substrate that had been coated on the back surface (and also on the edges) with ~1000Å of sputtered SiO_2 to attempt to prevent any interaction of the Ge substrate with the MO-CVD environment after initiation of GaAs deposition. This wafer was then fabricated into small-area mesa diodes and their properties were compared with those of similar devices grown on the uncoated Ge substrates. Improved results were achieved, so the procedure of coating Ge substrates to be used in the GaAs MO-CVD environment appeared to be a helpful one and thus was used for most Ge substrates involved in GaAs depositions throughout the remainder of the program.

In the subsequent series of deposition experiments several GaAs thin-window cell structures were grown simultaneously on n-type (Sb-doped) (100)-oriented Ge and n-type (Si-doped) (100)-oriented GaAs substrates by the MO-CVD process.

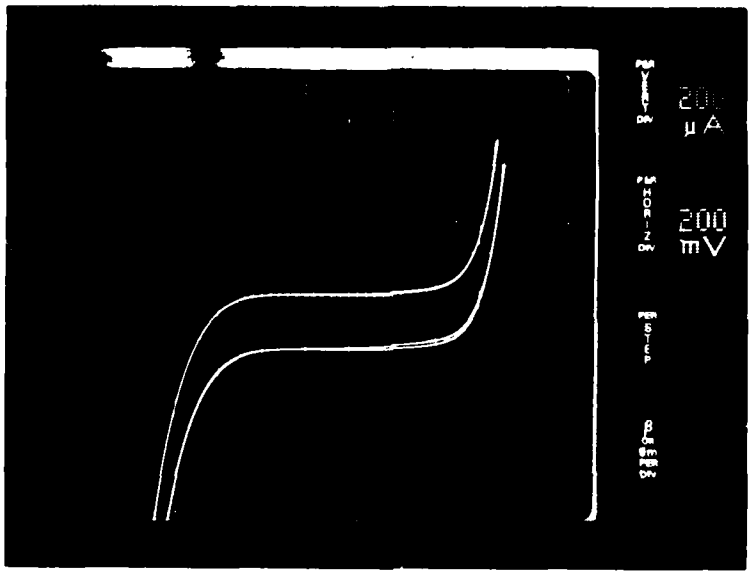
These structures were deposited at 700, 750, and 800°C. A few of the Ge substrates had been previously coated with ~1000Å of sputtered SiO_2. In addition, some GaAs p-n junction structures without GaAlAs window layers were grown on Ge:Sb substrates (some SiO_2-coated and some uncoated). The cell structures were processed into 0.5cm x 0.5cm devices, while the simple junction structures were fabricated into small mesa diodes.

In general, the solar cells and junction diodes fabricated in GaAs grown on SiO_2-coated Ge substrates in this group exhibited less leaky I-V characteristics than those on uncoated Ge substrates. However, all of the solar cells grown on Ge substrates (coated or uncoated) had V_{oc} values of only ~0.8V under illumination by a laboratory microscope lamp, whereas cells grown on GaAs substrates typically exhibited V_{oc} values of ~0.96V under the same illumination conditions. The cause of this difference was not established at the time.

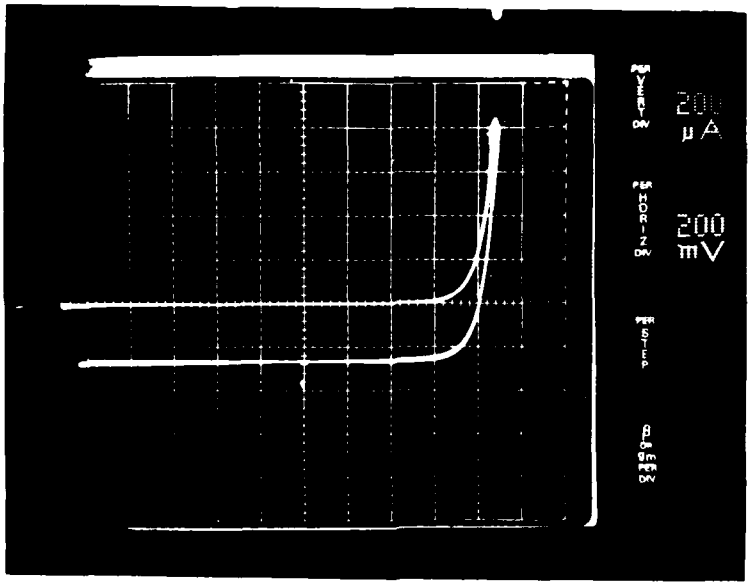
Figure 25a shows the dark and illuminated (microscope lamp) I-V characteristics of a GaAs p-n junction mesa diode (no GaAlAs window layer) grown on a Ge substrate that was uncoated. Figure 25b shows similar curves for a similar device grown on a Ge substrate having the SiO_2 coating (except on the deposition surface). The 50 mil x 50 mil mesas had centrally located 25 mil x 25 mil ohmic contacts on their top surfaces, as for earlier mesa devices.

Some of the samples in the above group were not processed into devices until the following month, at which time they were processed into the standard-size cells with other, more recently grown, samples. Upon testing with the 1kw xenon lamp (simulated AM0 illumination) it was found that the cells on GaAs again had higher efficiencies than those grown simultaneously on Ge. Figure 26a shows the AM0 photoresponse of one of these cells grown on GaAs:Si and Figure 26b shows the dark and light I-V characteristics of a cell in the simultaneously grown multilayer structure on SiO_2-coated Ge:Sb. These cell structures were grown at 700°C. No AR coatings were used and no allowance was made in calculating the efficiencies for the area shielded by the contact grid. The efficiency of the cell on the Ge substrate is seen to be less than half of that of the cell on the GaAs substrate, primarily due to significantly lower I_{sc} and V_{oc} values although even the fill factor is better for the GaAs-based cell (0.80) than for the Ge-based cell (0.70).

Some attempts were then made to identify the possible cause(s) of these persistent differences. Semilogarithmic plots of current vs voltage were made for some of the devices to compare the junction properties of the GaAs-based and the Ge-based cells and to compare both with those of similar cells grown earlier in the program. Figure 27a shows the forward (dark) I-V characteristic of a GaAlAs-GaAs solar cell structure grown on a GaAs:Si substrate and processed into a completed device with this later group. Figure 27b shows the corresponding data for a similar cell on a GaAs:Si substrate grown and processed several months earlier. (In both instances the data were obtained with the automatic plotter.) It is evident that the more recent cell shows considerably more leakage at low voltages. The current conduction appears ohmic at zero bias, suggesting a severe shunting problem. It was not established at the time whether this shunting was related to device fabrication or materials growth problems.



(a)



(b)

Figure 25. Dark and Illuminated I-V Characteristics of GaAs p-n Junction Mesa Diodes (50 mil x 50 mil) Grown by MO-CVD on n-type (100)Ge Substrates; a) Uncoated Substrate; b) Substrate Coated with SiO_2 (Microscope lamp source; 25 mil x 25 mil central contact on top surface of device)

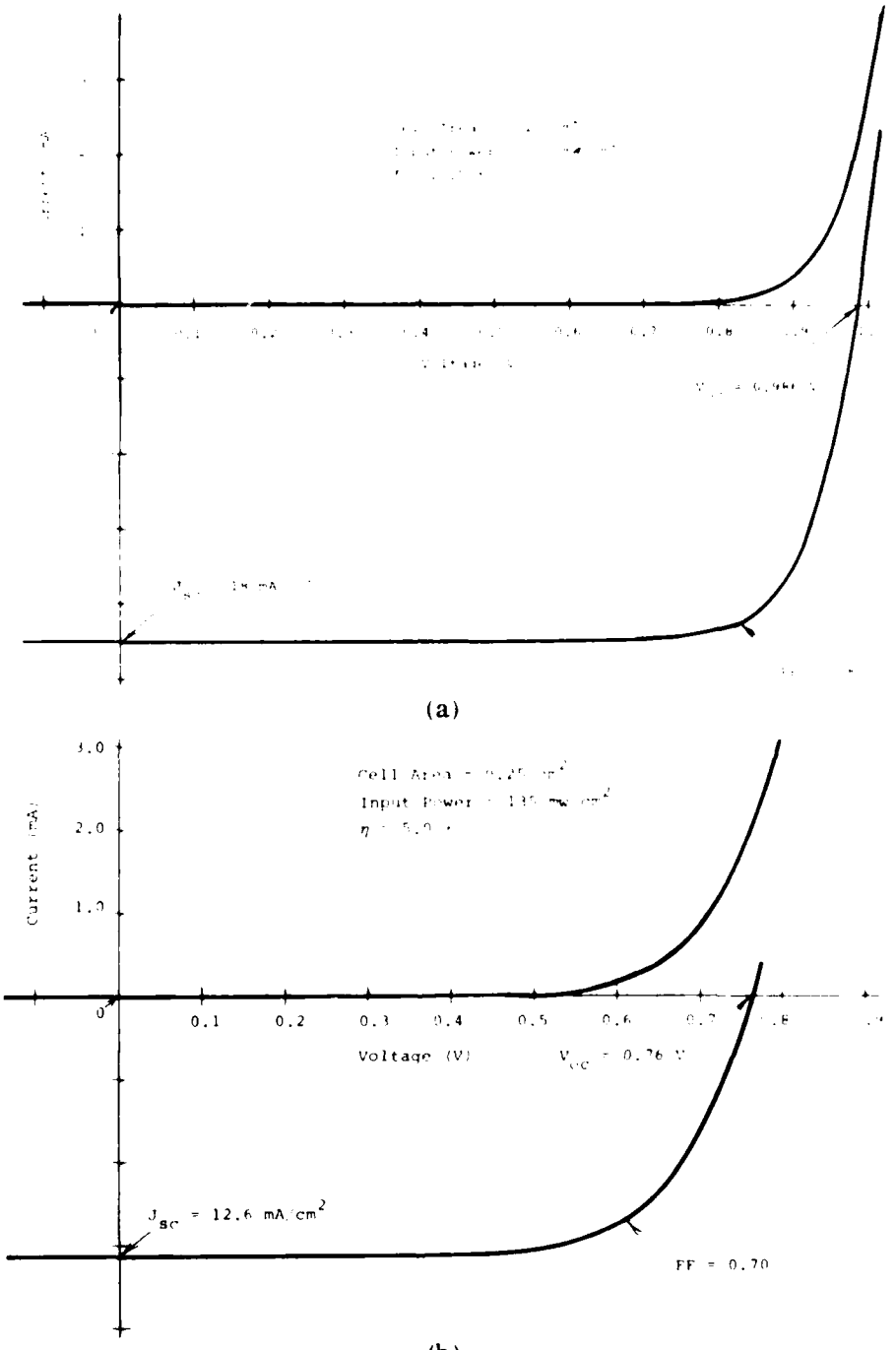
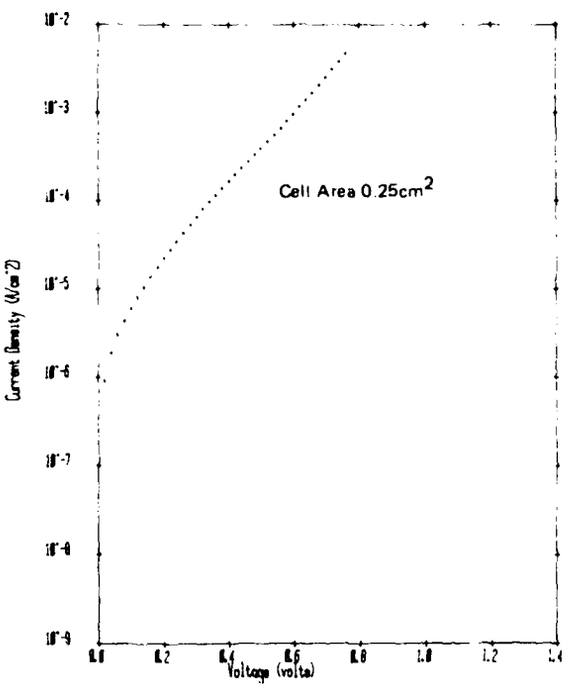
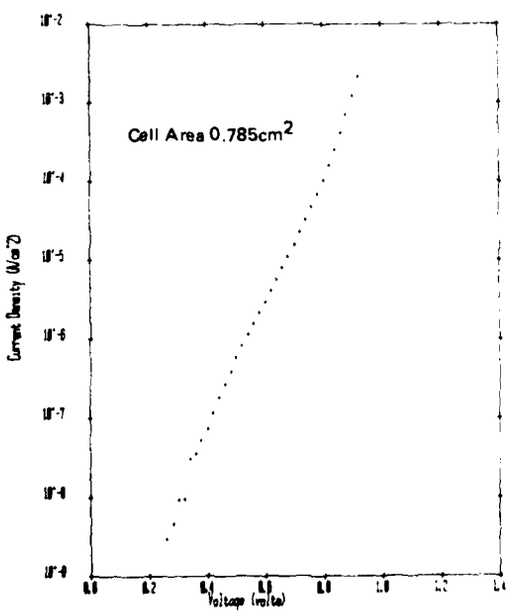


Figure 26. Dark and Illuminated I-V Characteristics of GaAlAs-GaAs Solar Cells Grown by MO-CVD at 700°C Simultaneously on a) Single-crystal (100)GaAs:Si Substrate and b) Single-crystal (100)Ge:Sb Substrate with SiO_2 Coating



(a)



(b)

Figure 27. Forward Dark I-V Characteristics of GaAlAs-GaAs Solar Cells Grown by MO-CVD on GaAs:Si Substrates and Processed into Completed Devices a) in Sixth Month of Program and b) Early in Program

While these investigations were in progress additional groups of GaAlAs-GaAs heteroface cell structures were prepared, with n-type (Sb-doped) (100)Ge and n-type (Si-doped) (100) GaAs substrates included for simultaneous deposition in each run. One group was deposited entirely at 700°C, and all of the Ge substrates were coated with ~1000Å of sputtered SiO_2 on the back surface. A second group involved deposition temperatures of 650 and 700°C, again with the Ge substrates all previously coated with SiO_2. Several separate runs were also made to grow similar cell structures just on GaAs:Si substrates alone at 750°C, for comparison.

Some of the samples of the first of the above groups, grown at ~700°C on both GaAs and Ge (SiO_2-coated) substrates, were processed separately into 0.5 cm x 0.5cm cells and were tested in individual chip form with probe contacts and the microscope lamp. Representative dark and illuminated I-V curves for several of these cells are shown in Figures 28 and 29.

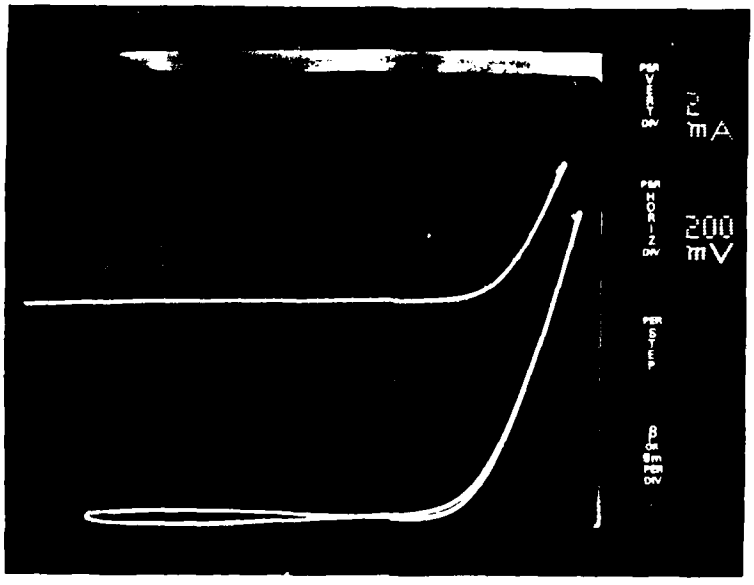
Figure 28a shows the I-V curves of a GaAlAs-GaAs cell grown on (100)Ge:Sb at 690°C. The cells from this wafer were unique in that they were the first of the cells grown on Ge substrates in this program to show high values of V_{oc}. Also, they showed relatively small leakage currents. The companion GaAlAs-GaAs cells grown simultaneously on GaAs:Si substrates also exhibited good I-V curves, as shown in Figure 28b.

Figure 29a shows a similar GaAlAs-GaAs cell grown on a Ge:Sb substrate at ~700°C, but the initial (i.e., predeposition) conditions used in the growth of the GaAs layer in this case were different from the conditions used for the growth of the cell structures represented in Figure 28. The V_{oc} of the Ge-based cell in Figure 29a is much lower than that of the cell in Figure 28a.

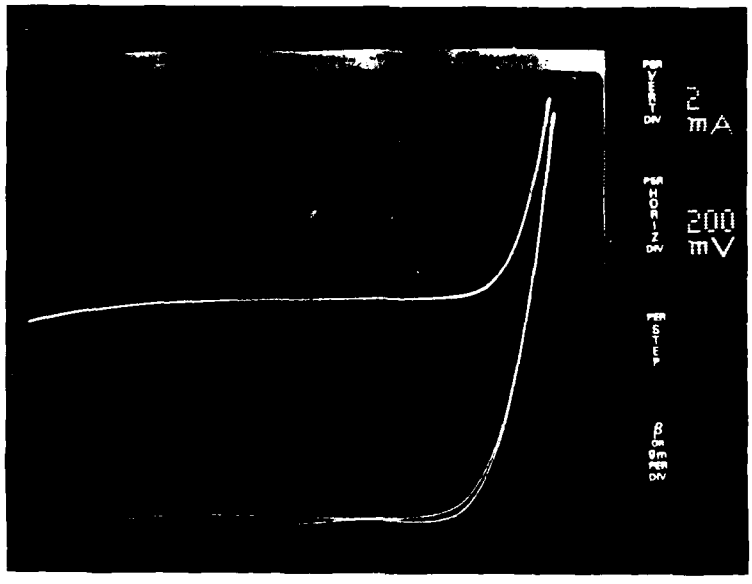
The companion cell grown on GaAs:Si simultaneously with the one shown in Figure 29a, however, has a good V_{oc}, as shown in Figure 29b, but its leakage current is seen to be higher than that in the cell of Figure 28b.

The question of the effect of changes in the predeposition conditions in the reactor, as employed in preparation of these samples, was examined further. The normal procedure for GaAs growth on GaAs substrates by MO-CVD is to introduce AsH_3 into the deposition chamber several minutes prior to the introduction of the TMG. Some of the GaAs films (Figure 28) were grown by this standard procedure and others (Figure 29) were deposited with the AsH_3 being introduced only a few seconds ahead of the TMG, thus avoiding the formation of uncombined Ga metal inclusions at the interface yet reducing the time for Ge-AsH_3 reactions to occur.

A separate set of undoped GaAs films was deposited at ~700°C on (100)-oriented n-type Ge:Sb substrates that had previously been examined by x-ray transmission topography so that structural characteristics of the GaAs films could be correlated with structural properties of the Ge substrates. Some of the films were grown with the standard predeposition procedure and some with the short AsH_3 exposure, to attempt to identify any structural differences in the films for the two types of substrate surface treatment. Additional window-type GaAs cell structures were grown on (100) GaAs and (100) Ge substrates simultaneously at ~750°C for use in this investigation; several were prepared with the standard procedure and others with the modified procedure.



(a)



(b)

Figure 28. Dark and Illuminated (microscope lamp) I-V Characteristics of GaAlAs-GaAs Heteroface Solar Cells (0.25 cm^2 area) Grown by MO-CVD at ~690 C on a) (100) Ge:Sb Single-crystal Substrate and b) (100) GaAs:Si Single-crystal Substrate.

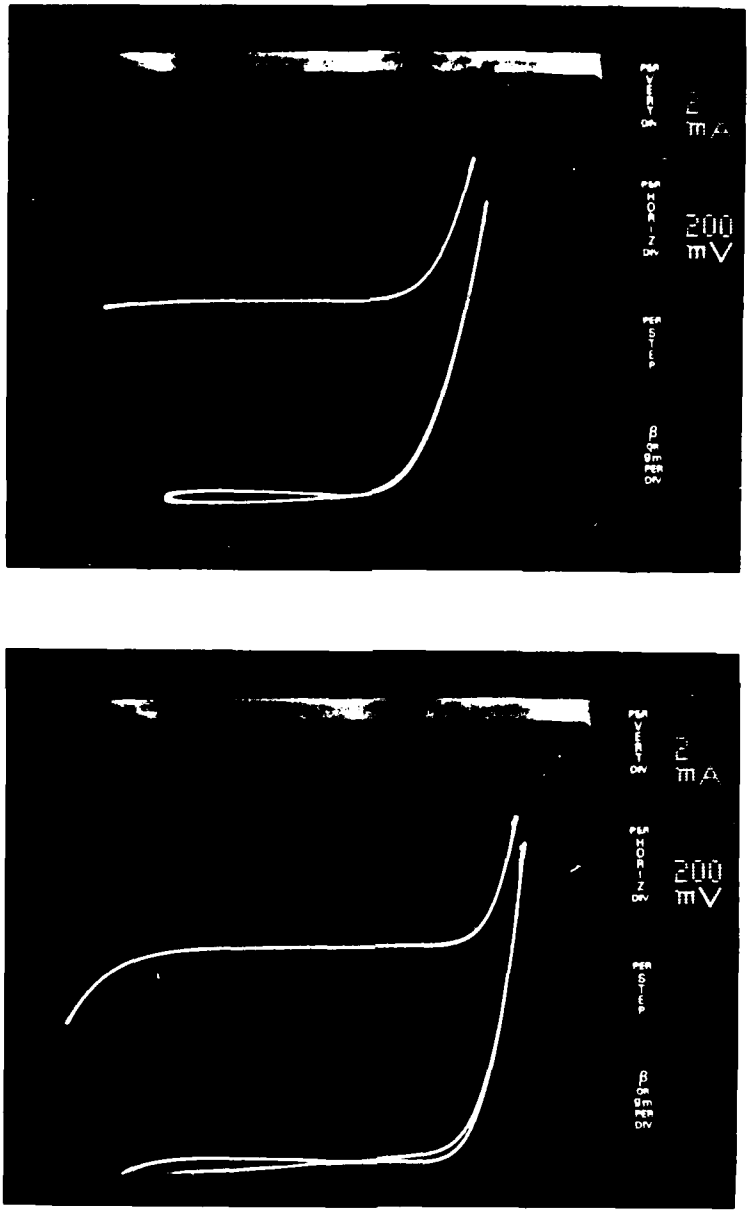


Figure 29. Dark and Illuminated (microscope lamp)I-V Characteristics of GaAlAs-GaAs Heteroface Solar Cells (0.25 cm^2 area) Grown by MO-CVD at ~700°C on a) (100) Ge:Sb Single-crystal Substrate and b) (100) GaAs:Si Single-crystal Substrate, with Different Predeposition Conditions in Reactor Chamber from Those Used for Cells of Figure 28 (see text)

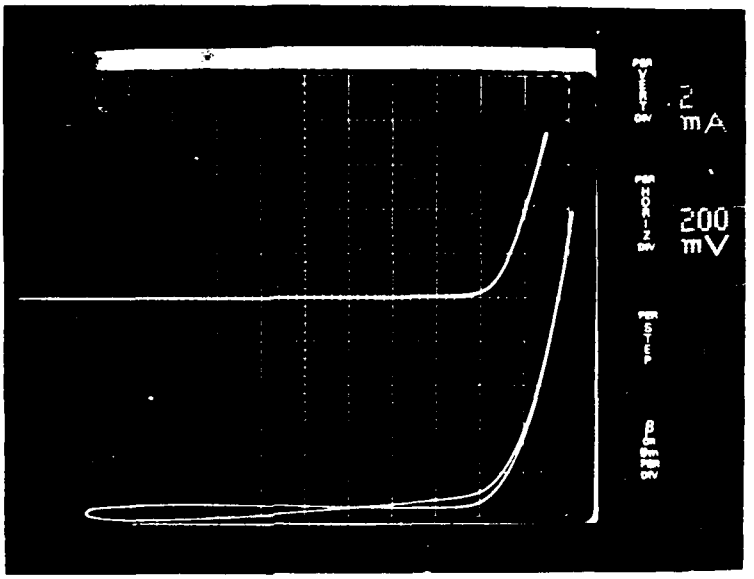
The GaAs films grown on Ge substrates with the standard predeposition procedure of introducing AsH_3 several minutes prior to the introduction of TMG tended to have a higher incidence of dislocations than those grown with the procedure variation in which the AsH_3 is introduced only a few seconds ahead of the TMG. The GaAs window-type cells grown at ~750°C on Ge substrates under the two different predeposition conditions also tended to exhibit different properties, with the cells grown with the standard procedure appearing to be inferior (especially in fill factor) to those grown with the non-standard procedure.

For example, GaAs cell structures grown at ~750°C simultaneously on substrates of Ge:Sb and GaAs:Si using the non-standard procedure were tested with the microscope lamp and probe contact procedure after being processed into arrays of individual cells, with results represented in Figure 30 for one of the deposition runs. Figure 30a shows the dark and illuminated I-V curves for a cell on the Ge:Sb substrate. A high V_{oc} value (>1.1V) was obtained, although the fill factor was not very high as displayed for this illumination intensity and method of contacting. The I-V curves for a cell on the companion GaAs substrate are shown in Figure 30b. A smaller V_{oc} was observed, but the fill factor was considerably better than that for the cell on Ge.

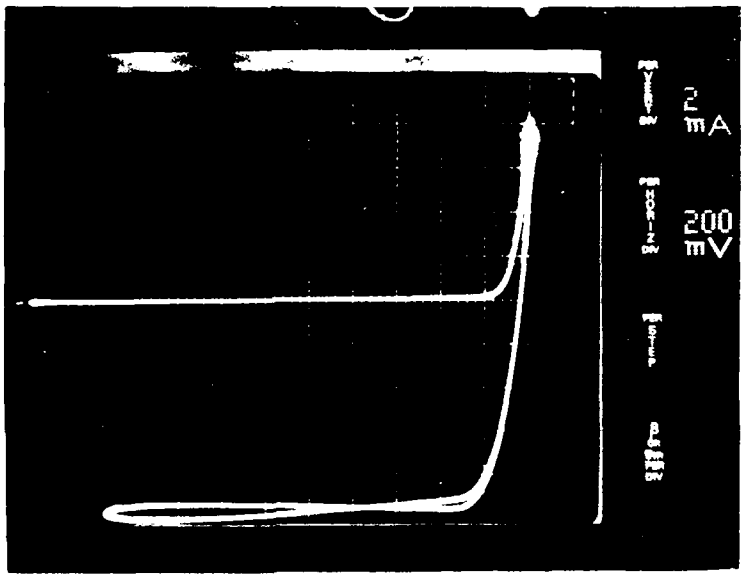
The I-V curves for a GaAs window-type cell grown on Ge:Sb at 750°C in a different experiment, in which the standard predeposition procedure was employed, are shown in Figure 31. Comparison of the curves in this figure with those in Figure 30a shows a high V_{oc} value in both cases, but the fill factor is clearly much poorer for cells grown with the standard predeposition procedure (Figure 31). The improved cell performance obtained with the nonstandard predeposition treatment appeared consistent with the observation of fewer dislocations in the GaAs films grown on Ge under these conditions.

Subsequent examination by x-ray reflection topography of three separate 0.5cm x 0.5 cm cells from the group involved in this examination of effects of predeposition treatment produced inconclusive results. Two of the cells were from the same original multilayer structure, which was grown with the standard predeposition procedure, while the third was from a sample grown with the modified procedure. Of the two cells from the same sample, one exhibited good dark and illuminated I-V characteristics and the other had poor photovoltaic properties (a phenomenon itself still not explained). However, the topographs from all three cells exhibited prominent "cross-hatching" or defect bands probably associated with stress-induced dislocation networks in the grown layers. Further analysis of carefully selected substrates and cell structures is required before significant correlations can be established by this method of analysis.

The I-V curves obtained with the AM0 simulator for another of the individual cells on the Ge:Sb substrate represented in Figure 31 (grown with the standard pre-AsH_3 procedure) are shown in Figure 32. The open-circuit voltage is seen to be slightly larger than that typically obtained with AM0 illumination for GaAs cells grown simultaneously on GaAs substrates, but a fill factor of only 0.65 was obtained, consistent with the low fill factor seen for the other cell on this substrate under microscope lamp illumination (Figure 31).



(a)



(b)

Figure 30. Dark and Illuminated macroscope Image I-V Characteristics of GaAlAs-GaAs Thin window Heterofface Solar Cells, [illegible] Grown by MO-CVD at 750°C Using "Non standard" Preferentation Procedure (see text) on a) Ge-Sb Substrate and b) GaAs-Si Substrate.

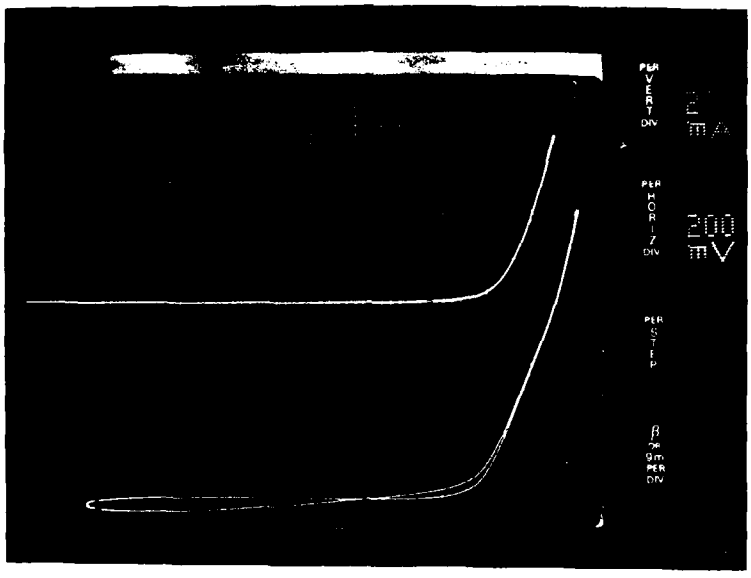


Figure 31. Dark and Illuminated (microscope lamp) I-V Characteristics of GaAℓAs-GaAs Thin-window Heteroface Solar Cell (0.5cm x 0.5cm) Grown by MO-CVD at 750°C on Ge:Sb Substrate Using Standard Predeposition Procedure

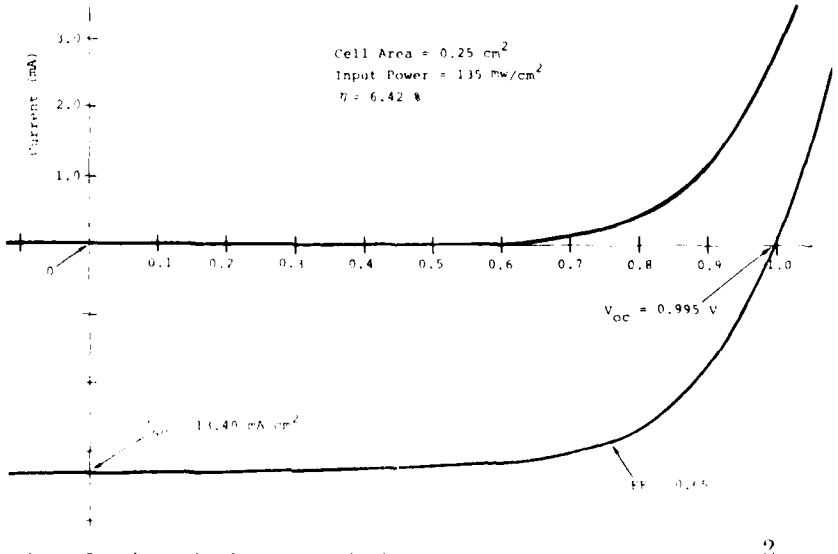


Figure 32. Dark and Illuminated (AM0 simulator, ~135 mw/cm^2) I-V Characteristics of Another GaAℓAs-GaAs Thin-window Heteroface Solar Cell (0.5cm x 0.5cm) Fabricated on Same Ge:Sb Substrate as Cell of Figure 31

The cause of the apparently enhanced open-circuit voltage being observed in these GaAs cells grown on Ge substrates was not identified at the time. It was speculated that an additional p-n junction formed inadvertently near the nominal Ge-GaAs interface could be responsible.

Subsequent further evaluation of some of these GaAs cell structures grown by MO-CVD on Ge substrates produced some interesting results. Measurement of the illuminated I-V curves (using the AM0 simulator) and of the spectral response curves for a number of the individual 0.5cm x 0.5cm GaAs cells on Ge substrates confirmed the earlier result that there was wide variation in the general photovoltaic quality of cells on a given Ge substrate, for structures prepared with either the nonstandard or the standard AsH_3 procedure. In fact, the variation of the V_{oc} values among the individual GaAs window-type cells on a given Ge substrate and among the individual cells on Ge and GaAs substrates used simultaneously in a given deposition experiment, as determined with AM0 illumination in these measurements, was found sufficiently large to dispel the previous impression that there was a consistent difference in V_{oc} values for cells on Ge and on GaAs substrates (with the former thought to be larger).

Furthermore, the cells in structures grown on GaAs substrates when Ge substrates were also present appeared, as a result of these later evaluations, to be generally poorer than GaAs window cells grown on GaAs substrates alone – a fact that cast considerable doubt on the validity of the earlier comparison of cells grown simultaneously on the two substrate materials. Further doubt was caused by the manner in which the microscope lamp illumination was employed in the rapid screening of cell properties – involving adjustment (by changing the lamp-to-sample distance) of the short-circuit current to ~10mA and then noting the resulting V_{oc} value and curve shape (fill-factor). Clearly, for cells with wide variations in series resistance, curve shape (fill factor), and overall quality this rapid-screening comparison method could be misleading.

Despite the wide variations found among individual cells in the group there were some good-quality GaAs cells found on the Ge substrates in structures prepared both by the standard and the nonstandard AsH_3 procedures. For example, Figure 33 shows the illuminated I-V curve for one of the heteroface cells grown at ~750°C on (100)Ge:Sb using the standard pre-AsH_3 procedure. The individual cell represented here is the same cell that produced the I-V curve of Figure 31 with microscope lamp illumination. Not only does this cell produce a normal open-circuit voltage of 0.99V but it also exhibits a good fill factor of 0.78 – significantly better than that shown in Figure 31. The J_{sc} for this cell under AM0 illumination, however, was only about 12.4mA/cm^2; this can be compared with a J_{sc} of 13.4mA/cm^2 for another individual cell on this same sample, which also had V_{oc} = 0.995V and FF = 0.65, as shown in Figure 32. The efficiency of the cell of Figure 33 was approximately 7.1 percent, while that of the cell shown in Figure 32 was 6.4 percent. Other cells on this same sample exhibited efficiencies up to ~7.9 percent in the AM0 measurements.

Figure 34 shows the illuminated I-V curve for one of the heteroface GaAs cells grown at ~750°C on (100)Ge:Sb using the nonstandard AsH_3 procedure, in an experiment in which GaAs substrates were also used. The V_{oc} value for this cell

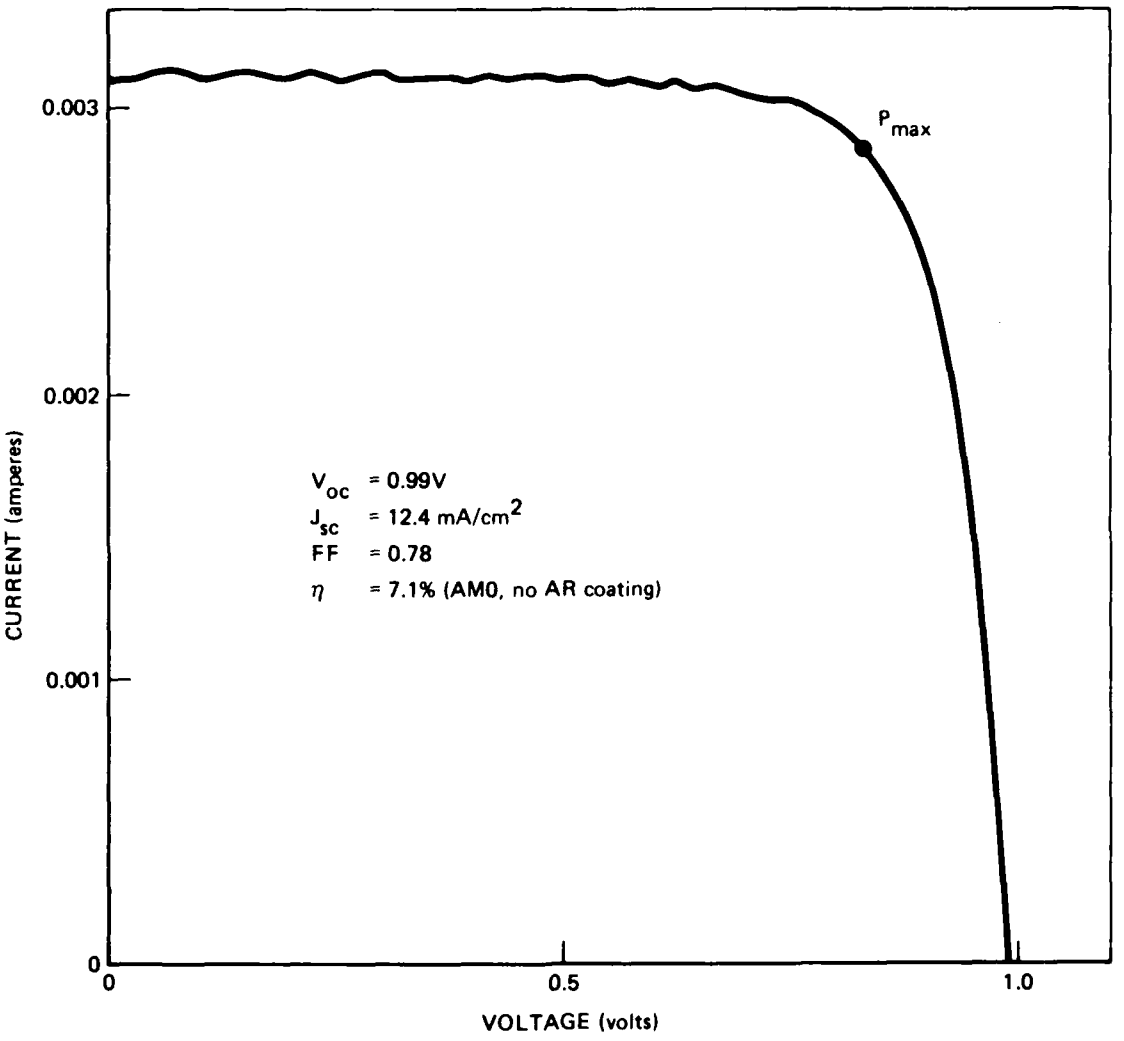


Figure 33. Fourth Quadrant of Illuminated (AM0 simulator) I-V Curve for MO-CVD GaAs Heteroface Solar Cell (0.5cm x 0.5cm) Grown at ~750°C on (100)Ge:Sb Substrate, Using Standard Pre-AsH_3 Procedure (Same cell as that which produced I-V curve shown in Figure 31)

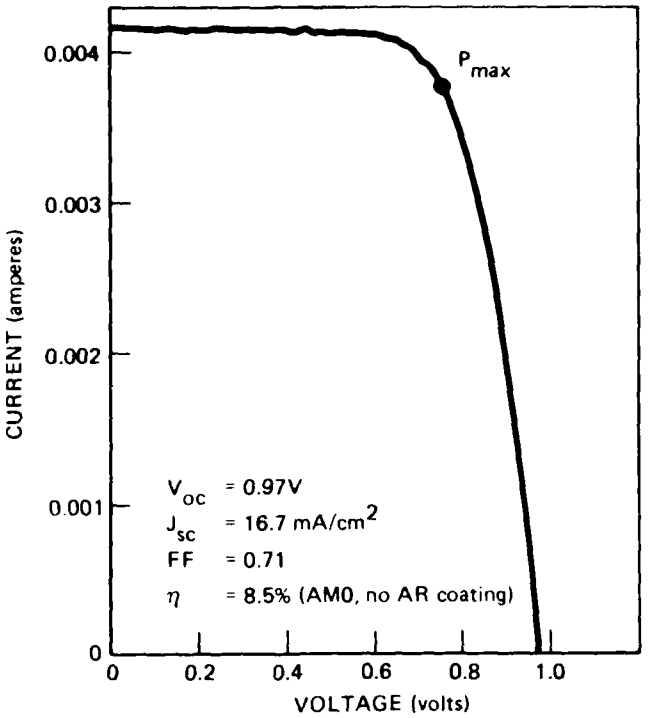


Figure 34. Fourth Quadrant of Illuminated (AM0 simulator) I-V Curve for MO-CVD GaAs Heteroface Solar Cell (0.5cm x 0.5cm) Grown at ~750°C on (100)Ge:Sb Substrate Using Nonstandard Pre-AsH_3 Procedure

is 0.97V, J_{sc} = 16.7mA/cm^2, the fill factor is 0.71, and the efficiency ~8.5 percent for AM0. The cell used to produce the I-V curve of Figure 30a, in which it had appeared that an unusually large V_{oc} had been generated by the microscope lamp illumination, was on this same sample and was found in these later AM0 measurements to produce a very low V_{oc} of only 0.76V, a J_{sc} of 9.7mA/cm^2, a fill factor of 0.70, and a power conversion efficiency of ~3.9 percent. Other cells on this sample had efficiencies up to 9.8 percent in the AM0 measurements.

In most instances the cause of the relatively low efficiencies was obviously the lower-than-expected photocurrent collected, indicating needed improvements in cell design -- primarily layer thicknesses and doping concentrations – and a possible problem with minority carrier diffusion lengths due to defects in the GaAs layers grown on the Ge substrates. The later measurements, however, did not indicate a clear-cut preference for either the standard or the nonstandard AsH_3 procedure for growing GaAs heteroface cells on Ge substrates.

The spectral response measurements made on these GaAs/Ge cells also indicated a lack of any long-wavelength response attributable to a possible second barrier involving Ge, except for two individual cells for which a very low V_{oc} (0.1 to 0.28V) was found and some long-wavelength response was detected. It is believed that the GaAs cell was completely penetrated by the contacts in the processing in these instances, so that either a GaAs-Ge heterojunction or a Ge Schottky-barrier cell resulted.

The possibility of obtaining improved GaAs cell performance on Ge substrates by growth at reduced temperatures was briefly explored by growth of a GaAs heteroface cell structure at ~660°C on a (100)Ge:Sb substrate; the substrate had been coated on the back with sputtered SiO_2 about 1000Å thick, as in previous experiments with Ge substrates. The individual ~0.5cm x 0.5cm cells processed on this sample exhibited generally poor dark and light I-V characteristics when examined with the microscope lamp and the probe contact, with considerable junction leakage evident and also evidence of excessive series resistance. When one of the cells was characterized with the AM0 simulator this general behavior was again observed. Under that illumination the V_{OC} was found to be only 0.68V, much lower than found for the other Ge-based cells described above (cf Figure 32). The observed J_{SC} was 13.2 mA/cm^2 and the fill factor was very low. Thus, even though this cell structure was prepared with the predeposition procedure that involved only very brief exposure of the substrate to AsH_3 before the TMG was admitted, it appeared that other things occurred at temperatures as low as 660°C to result in relatively poor quality growth of the cell structure.

Late in the Phase 1 program, at about the time the above AM0 measurements were being made on the GaAs/Ge cells grown earlier, additional GaAs window-type cell structures were grown on Ge:Sb substrates at ~700°C and on GaAs:Si substrates at ~750°C, with the standard pre-growth exposure for AsH_3 being used in several of the experiments and the nonstandard procedure of very brief exposure to AsH_3 being used in two of the runs. Figure 35 shows the spectral response curves for two of the heteroface cells of this group, one grown on GaAs and the other grown (in a separate deposition experiment) on Ge. The junction depth (p-type GaAs layer thickness) in the two cells was intended, by selection of deposition parameters, to be nominally the same. The large difference in blue response in the two cases suggests a major difference in the minority carrier diffusion length in the GaAs layers on the two substrate materials.

Unfortunately, however, the overall results obtained with this group of samples were decidedly inferior to those discussed above. Problems encountered in the functioning of the reactor system late in the Phase 1 program were apparently adversely affecting the properties of this group of cell structures, irrespective of the substrate material being used. Additional experiments with MO-CVD GaAs cell structures on either GaAs substrates or Ge substrates were thus delayed until early in the Phase 2 program.

It is clear that the GaAs cells produced on Ge substrates by the MO-CVD process in the Phase 1 program were of much poorer quality than those formed on GaAs substrates. It is believed that the device processing techniques that were used may have been responsible for some of the adverse effect, but other factors were probably more influential. The SiO_2 coating used on most of the Ge substrates should have prevented serious interaction of the substrate and the MO-CVD reactant atmosphere, although no attempt was made to evaluate critically the integrity of the SiO_2 layer or to determine an optimum thickness or deposition procedures.

Whereas clear evidence of a more defective GaAs-Ge interface region was found for structures grown with the longer-duration standard (as opposed to the very brief non-standard) exposure of the substrate to AsH_3, somewhat less conclusive results were obtained for the photovoltaic performance of cells in the two

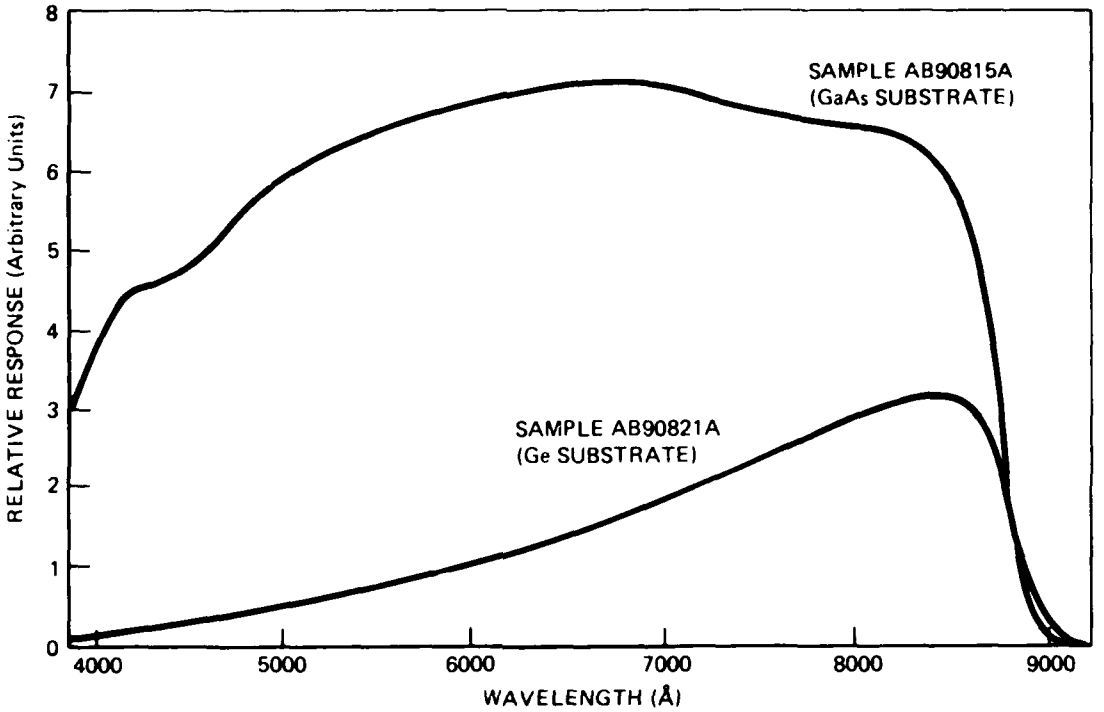


Figure 35. Spectral Response Curves for GaAs Heteroface Cells *Made by MO-CVD on GaAs and Ge Substrates;* Junction Depths Nominally Equal in Both Cells

cases – although the non-standard procedure is apparently preferable. Some additional investigation of this problem should be undertaken to clarify the matter.

The photovoltaic parameter in which differences among cells on GaAs and on Ge substrates were most noticeable was the short-circuit current density; open-circuit voltages and fill factors of the cells on Ge were usually reasonably high. The poor photocurrent collection that was consistently observed indicates a need for improved cell design (i.e., layer dimensions and impurity concentrations), a probable problem with minority carrier diffusion lengths in the defected GaAs layer adjoining the Ge, and possibly some difficulties caused by local inhomogeneities in the quality (structure and/or impurity content) of the Ge substrates. Also, no sharply defined preferred temperature range for growth of GaAs cells on Ge substrates emerged from the Phase 1 studies. The general conclusion is that the 700-750°C range is preferred over higher or lower temperatures, but there was little basis for any preference within that range.

2.2.2.3 MBE GaAs Cells on GaAs and Ge Substrates

The MBE process was employed in the fabrication of several different experimental cell structures in the Phase 1 program, but most use of this deposition technique was in the preparation of GaAs cell structures on both GaAs and Ge single-crystal substrates. This work is described in the next two subsections.

2.2.2.3.1 MBE GaAs Cells on GaAs Substrates. At about the time the modified Phase 1 program plan was being developed, the results being obtained in separately funded work with GaAs solar cell structures prepared by the MBE process at ERC Thousand Oaks were appearing very encouraging.

It should be noted that the MBE technique had been introduced earlier in the program as an alternate method for producing a connecting tunnel junction between LPE-grown GaAlAs and GaAs cells in the Task 5 investigations (see Section 2.5). It was also examined soon thereafter for possible use combined with the MO-CVD process to produce a hybrid tunnel junction between GaAlAs and GaAs cells. That tunnel junction structure involved an n^+GaAs layer deposited by MO-CVD on a p^+GaAs layer grown by MBE, and is described in Section 2.2.4.1.

The fourth quadrant of the illuminated I-V curve (AM0 simulator) obtained for a heteroface GaAlAs/GaAs solar cell grown by MBE on GaAs at a substrate temperature of ~580°C late in Phase 1 is shown in Figure 36. The observed open-circuit voltage of 0.94V and the fill factor of 0.84 indicate the good quality GaAs cells that were made by this deposition technique, despite the moderate short-circuit current density (17.2 mA/cm^2) realized. The AM0 efficiency of this cell was 10.1 percent, with no AR coating.

2.2.2.3.2 MBE GaAs Cells on Ge Substrates. The relatively low substrate temperatures required for growth of GaAs layers by the MBE process make the technique attractive for use with substrate materials such as Ge. Some preliminary experimental GaAs cell structures were grown by this technique on Ge substrates late in the Phase 1 program.

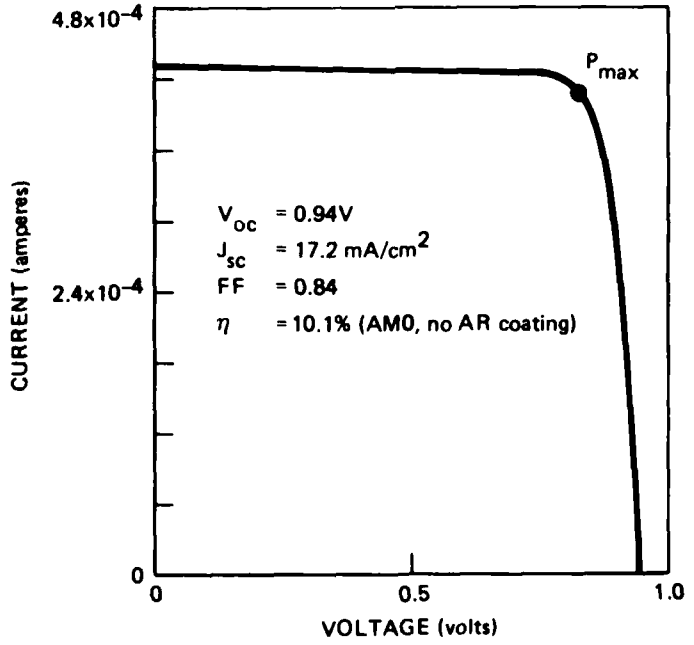


Figure 36. Illuminated (AM0 simulator) I-V Curve for GaAs Heteroface Solar Cell (area 0.025 cm^2) Grown by MBE at ~580°C on (100) GaAs Substrate

Initial attempts to produce suitable GaAs layers by MBE on etched p-type Ge wafers were only partially successful. Subsequent attempts, however, which included hypochlorite optical polishing of the Ge wafers followed by CP-4 etching and an in-chamber sputtering treatment of the substrate at the initial GaAs deposition temperature (~640°C), produced GaAs layers of excellent quality on Ge. The film surfaces were mirror-like and the films exhibited background doping concentrations of $\sim 10^{16}$ cm^{-3}. Some of the initial GaAs MBE layers on n-type (100) Ge substrates were doped sequentially to produce n-p junctions in the deposited structures. This resulted in the typical series of I-V traces shown in Figure 37 for several different illumination intensities obtained with the microscope lamp. The family of curves shown is reminiscent of those typical of a conventional junction transistor connected in the common-emitter configuration, with collector current plotted vs collector-emitter voltage and with base current as a parameter. (The variation in level of illumination in the figure would correspond to the parametric base-current variation for the transistor.)

The spectral response curve for such a structure is shown in Figure 38. The general shape of this curve is consistent with that of a device made up of an nGaAs region on a pGaAs region adjacent to a pGaAs-nGe heterojunction. The pattern of maxima and minima superimposed on the Ge portion of the photoresponse is caused by multiple-beam interference effects in the thin GaAs layer on the Ge substrate. The interfringe spacing is related to the GaAs layer thickness while the magnitude of the fringe peak heights (actually the ratio of adjacent maxima and minima) is a function of the reflectivity at the GaAs-Ge interface and at the air-GaAs interface.

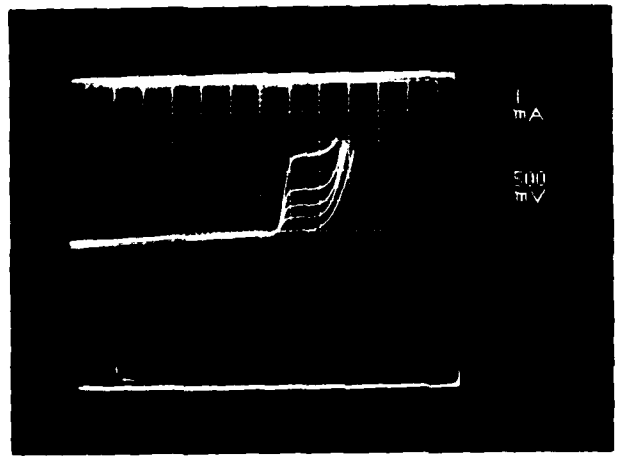


Figure 37. Illuminated I-V Curves for GaAs n-p Solar Cell Structure (area 0.025 cm^2) Grown by MBE on n-type (100) Ge Substrate, for Several Different Levels of Illumination from Microscope Lamp

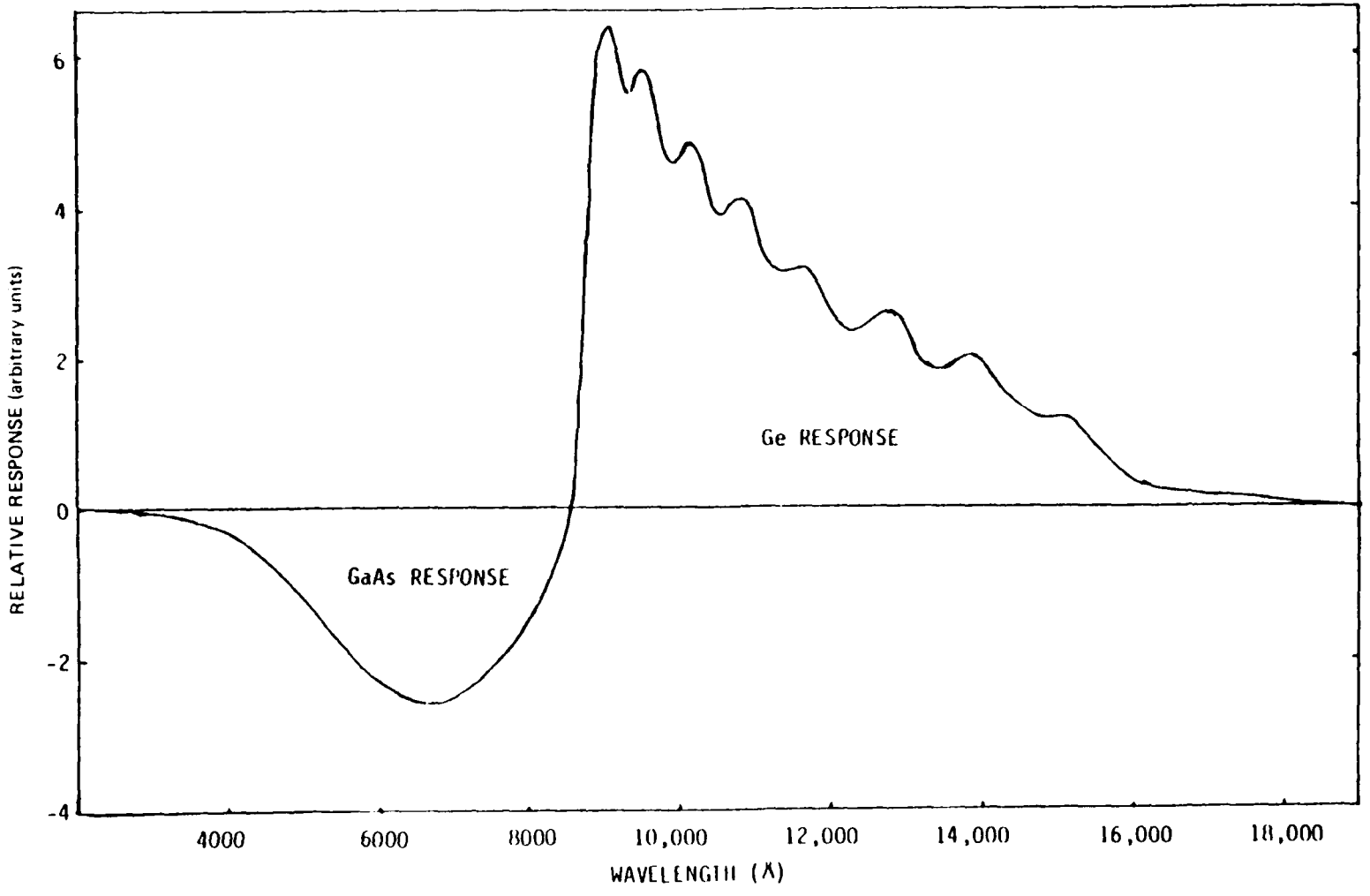


Figure 38. Spectral Response Curve for MBE-grown Device of Figure 37, Showing Photoresponse of Opposite Sense for n/p GaAs Junction and pGaAs-nGe Heterojunction

Using the standard expression relating film thickness, film material refractive index (3.6 for GaAs in this spectral range), and spacing between adjacent maxima (or minima) in the interference pattern, it was found that the (calculated) thickness of the GaAs in this sample was 2.2 μm, in excellent agreement with the thickness expected on the basis of the MBE deposition parameters. Similarly, the reflectivity at the GaAs-Ge interface was calculated from the ratios of adjacent maximum and minimum intensities, "normalized" to a single wavelength to remove the effect of variation in background spectral response with wavelength. This calculation led to a value for the Ge dielectric constant at $\lambda \sim 0.9\,\mu m$ of $\epsilon_{Ge} \quad \tilde{n}^2_{Ge} \quad 15.673$, where $\tilde{n}_{Ge} \quad n_{Ge} - i\kappa_{Ge}$. This value is in reasonable agreement with literature values for ϵ_{Ge} of 15 to 16.5 for this wavelength range.

Additional GaAs cell structures were being grown on Ge substrates under various MBE deposition conditions at the conclusion of the Phase 1 program, and the work is expected to be expanded in Phase 2.

2.2.3 Ge Solar Cells for GaAs-Ge SMBSC's

The two configurations considered for the GaAs-Ge two-cell SMBSC involve 1) deposition of an epitaxial Ge solar cell structure on a GaAs single-crystal substrate in or on which the GaAs cell is formed, and 2) deposition of an epitaxial GaAs solar cell structure on a Ge single-crystal substrate having the Ge cell on it or in it.

One of the main concerns about the first configuration relates to the small optical absorption coefficient for Ge in the wavelength region 1.5-1.7μm, the value decreasing abruptly from ~4500 cm^{-1} at 1.5 μm to ~30 cm^{-1} at 1.7 μm (at room temperature). Thus, absorption of all or most of the available photons in this wavelength region would require a large Ge thickness, perhaps too large for practical growth by the CVD process. On the other hand, the fraction of the total usable solar photons that is in this band is not large, and it may not be practical to attempt to collect the carriers generated by them even in a bulk Ge solar cell.

This question was addressed in Task 1 of the Phase 1 program, as discussed in Section 2.1.2, with the conclusion that the maximum short-circuit current obtainable with a Ge solar cell occurs for a thick cell with a back-surface field. Thus, the second configuration, involving use of a Ge single-crystal substrate, appeared more promising.

Despite these concerns, both configurations received attention in the Phase 1 program. The first configuration obviously depends heavily on development of satisfactory procedures for growing epitaxial Ge cell structures on GaAs single-crystal wafers or films. The second configuration requires GaAs epitaxial cell structures grown on Ge single-crystal wafers or films, the investigations of which have been described in part in Section 2.2.2. Relative to the second configuration, consideration was given to the possibility of using other cell fabrication techniques than thin-film deposition methods for formation of the Ge cell structures on which to grow the epitaxial GaAs cells; for example, ion implantation methods or conventional thermal diffusion of impurities applied to bulk Ge single-crystal wafers could provide the structures on which to grow the GaAs epitaxial film cells to achieve tanem cells. Only thermal diffusion was pursued experimentally in Phase 1, and that only briefly.

The preparation of Ge solar cell structures by CVD [illegible] methods, and by thermal diffusion processes is described in the following three subsections.

2.2.3.1 Ge Solar Cell Structures by CVD

The GeH_4 pyrolysis reaction in an H_2 atmosphere at temperatures in the range 550-850°C was selected for use in producing Ge films by CVD for solar cell structures. Ge deposition experiments with this process were begun in the fifth month of the program, employing a reactor system that had been designed and was mainly used for the growth of GaAs and GaAlAs by the MO-CVD process.

The first expitaxial Ge p-n junction structures were grown on Ge:Sb substrates in this system. The n-type layers were deposited undoped, which for the reactor system and GeH_4 source being used resulted in a background doping concentration of 1-3 x 10^{17} cm^{-3}, a relatively high and not satisfactory level. The p-type layers were Ga doped, using TMG as a dopant source. Typically, the junction structures were grown with p layers ~1 μm thick and n layers ~5 μm thick.

Some of these samples were processed into 50 mil x 50 mil mesa diodes having 25 mil x 25 mil top contacts centrally located. The dark and illuminated (microscope lamp) I-V curves of one of the early devices are shown in Figure 39. The large leakage current typical of these first devices is clearly shown. It was probably associated with the heavy p-type and n-type doping concentrations in the regions forming the junctions.

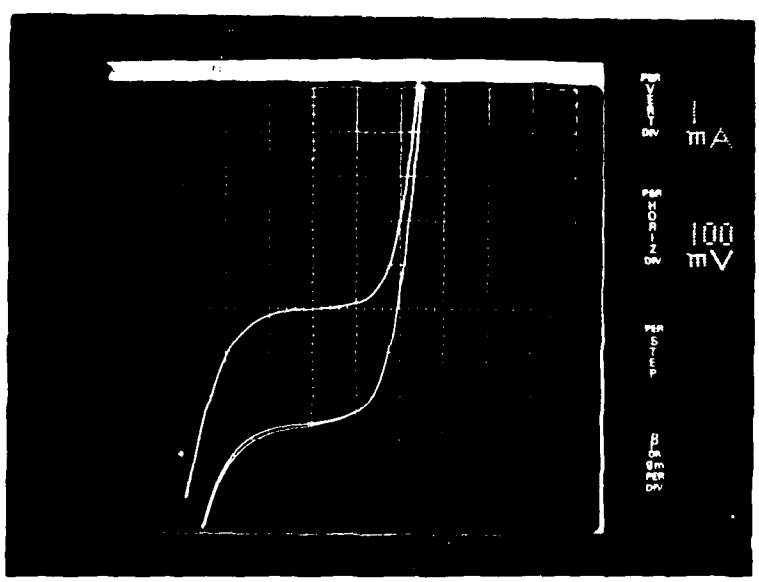


Figure 39. Dark and Illuminated (microscope lamp source) I-V Characteristics of Ge p-n Junction Mesa Diode Grown by MO-CVD on Single-crystal Ge:Sb Substrate (Mesa 50 mil x 50 mil, with 25 mil x 25 mil central contact on top surface)

Soon after these initial results were obtained, the GeH$_4$ source was transferred from one MO-CVD reactor to another one that was equipped with mass flow controllers, thus permitting better control over the Ge deposition conditions. To determine the background doping concentration and the degree of doping concentration control achievable with the second system a series of epitaxial films of n-type and p-type Ge was grown on high-resistivity, single-crystal (100)Ge substrates.

The undoped films were n type, as obtained in the first reactor, with $n \sim 1 \times 10^{17}$ cm^{-3}. It was concluded that the high unintentional doping concentration was probably caused by the GeH$_4$ source itself; unfortunately, this source gas was available at that time only in relatively poor purity (≈99.9 percent). Acceptor doping was accomplished by the addition of TMG to the reactant gas stream during growth of the Ge layers to introduce Ga into the layers, as had been done in the other reactor system. Since control of the background (n-type) doping concentration appeared to be difficult, at least for the particular GeH$_4$ source in use, it was planned at that time to prepare some Ge p-n junctions by conventional thermal diffusion processes for use in solar cell fabrication. Those efforts are described in Section 2.2.3.3.

Additional Ge p-n junction structures were grown epitaxially on (100)Ge:Sb single-crystal substrates in the second reactor system and processed into 0.5 cm x 0.5 cm solar cell devices. Typical dark and light I-V characteristics for these devices are shown in Figure 40. A microscope lamp was used for

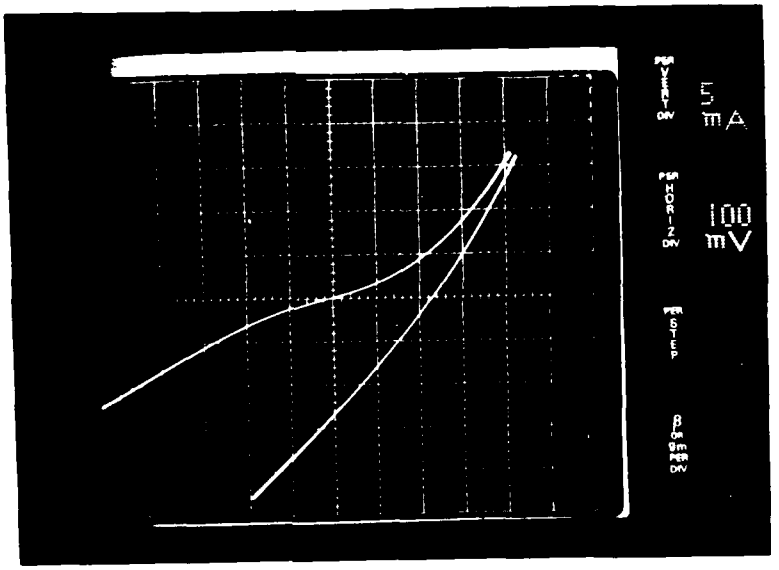


Figure 40. Dark and Light (microscope lamp source) I-V Characteristics of Ge p-n Junction Solar Cell Grown by GeH$_4$ Pyrolysis on Single-crystal (100)Ge:Sb Substrate (Cell 0.5 cm x 0.5 cm, with finger-grid top contacts)

illumination. The diodes were again quite leaky, as shown, probably again due to the relatively high doping concentration in the p and n layers forming the junction. Not all of the epitaxial Ge junction structures were that leaky; a few of them exhibited I-V characteristics as shown in Figure 11. However, the forward voltage of these diodes was very low, as shown, probably because of a graded junction being formed rather than an abrupt junction.

In the seventh month of the program the Ge deposition experiments were transferred from the MO-CVD reactor system to another reactor system — one that was completely free of Ga and As impurities and used prior to that time only for Si deposition experiments. This was expected to reduce the background doping concentration found in the Ge layers by a significant amount.

The first Ge films grown in this reactor were deposited on 10 ohm-cm n-type Ge substrates obtained from Eagle-Picher Co. and polished by Rockwell ERC. Experimental growth of undoped films at ~750°C on these substrates resulted in both films and substrates that were found to be entirely p type. It was suspected that these results were manifestations of the thermal conversion process (to p type) known to occur in high-resistivity n-type Ge exposed to temperatures above 700°C for extended periods. That this was indeed the case was verified by several experiments in which the Ge substrate material was cycled to "deposition temperatures"

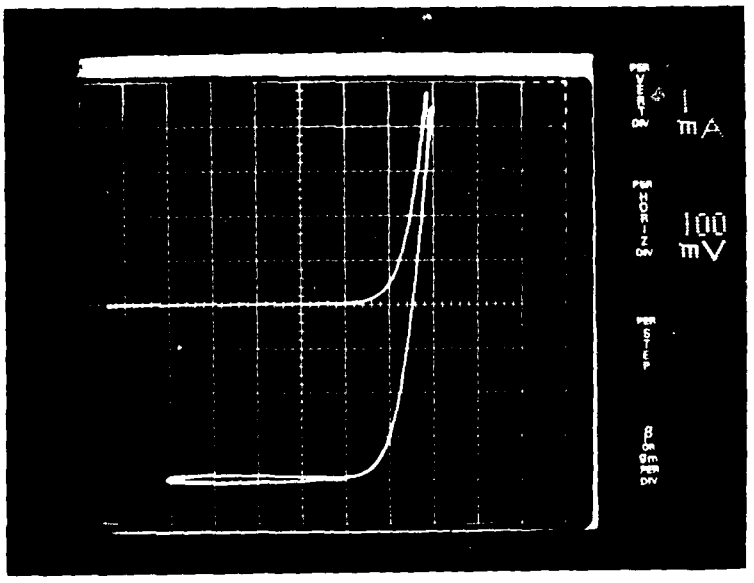


Figure 11. Dark and Light (microscope lamp source) I-V Characteristics of Ge p-n Junction Mesa Diode Grown by GeH_4 Pyrolysis on Single-crystal (100)Ge:Sb Substrate (Mesa 50 mil x 50 mil, with 25 mil x 25 mil central contact on top surface)

of 750°C and 650°C but without any actual deposition. No conversion of the substrate occurred at 650°C, and it was also determined that undoped Ge layers that were also n type could be grown at that temperature. Subsequent Ge CVD experiments using the GeH_4 pyrolysis were thus carried out at ~650°C. It should be noted that Ge films of good quality had been grown by the GeH_4 process earlier in the program at higher temperatures – e.g., 850°C – but because of the combining of Ge and GaAs structures in the SMBSC it is desirable to prepare the structures at temperatures as low as possible and avoid disturbing previously prepared impurity distributions.

Deposition of Ge at ~650°C resulted in reduced film growth rates relative to those achievable at higher temperatures; a maximum of 900-1000 Å/min was realized. Layers doped p type by addition of boron, obtained by introduction of diborane to the reactant gas stream, were prepared in a range of impurity concentrations (i.e., carrier concentrations). By alternating undoped (n-type) and B-doped (p-type) layers it was possible to prepare several different junction structures on both Ge and GaAs substrates. Specifically, p/n Ge structures were grown on n-type Ge substrates and on n-type GaAs substrates at ~650°C. Typically these structures, evaluated by van der Pauw measurements of Hall effect and by spreading resistance probe scans, consisted of a p-type top layer 1-5 μm thick with a hole concentration of $1\text{-}4 \times 10^{19}$ cm^{-3} and hole mobility of ~200 cm^2 V-sec on an undoped n-type layer about 10 μm thick with resistivity the order of 10^{-2} ohm-cm.

Figure 42 shows the reduced-data plot of computer-calculated resistivity versus depth into the sample for a double-layer Ge film grown by CVD on a substrate of n-type (100)-oriented GaAs:Te at a temperature of ~670°C and analyzed by the spreading resistance technique.* The plot uses the symbols "P" to indicate p-type conductivity and "N" to indicate n-type material, information confirmed separately by an automatic scan of the same sample region with a recording thermoelectric probe (data not shown in the figure). The raw spreading resistance (SR) probe scan data are automatically corrected by the apparatus using values obtained in measurements on single-crystal standard bulk samples of known resistivity and the appropriate crystallographic orientation. Corrections are also automatically included for the finite sampling volume of the double probe. The scan is made on a beveled surface, in this instance a plane at an angle of 0.01 rad (~0.5 deg) below the top surface of the sample, with 10 μm distance (along the beveled surface) between successive readings.

The first-grown layer of this sample was undoped (n-type) Ge of nominal thickness 7.5 μm; the SR scan, which was not carried completely to the Ge-GaAs interface, indicates a thickness of something in excess of 5 μm and a resistivity of ~0.025 ohm-cm. The second layer was B-doped (from B_2H_6) during growth and had a nominal thickness (from known growth rate data) of ~5 μm; the SR scan shows t ≈ 5.0 μm and a resistivity that varies from ~0.045 ohm-cm at the interface to ~0.005 ohm-cm at the surface of the sample.

*Spreading resistance measurements were made by Solecon Laboratories, Inc., Costa Mesa, CA.

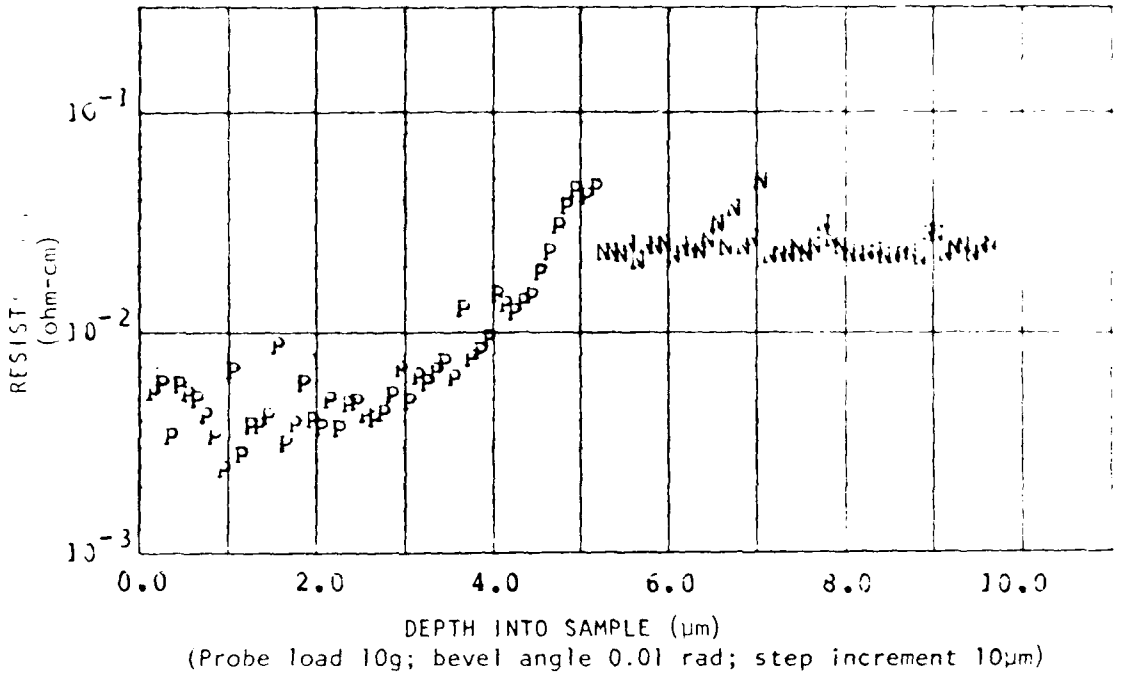


Figure 42. Resistivity as Function of Depth into Sample as Obtained by Spreading Resistance Probe Scan on Beveled Surface in Two-layer CVD Ge Film Grown at 650°C on n-type GaAs Surface; p-n Junction Shown Is at Interface between p-type and n-type Ge Layers

Similar measurements on the Ge CVD layers grown on high-resistivity n-type Ge substrates confirmed the thermal conversion to p type of that substrate material when the film was deposited at 750°C but its remaining n type when the film was deposited at 650-660°C. The SR technique was found to be a useful method of measurement for certain types of sample that are not conducive to other techniques of conductivity-type determination or transport property measurement.

The as-grown Ge layer surfaces on some of these samples were not very smooth and reflective, as if the (100)-oriented substrate growth surfaces had been improperly cleaned or somehow contaminated after placement in the deposition chamber. This applied to films on both Ge and GaAs substrates. Consequently, the substrate cleaning procedures were carefully reviewed, the reactor system was checked thoroughly for leaks, and a brief examination of the effects of substrate crystallographic orientation was made to attempt to identify the cause of the relatively poor surface quality.

The cleaning procedures were judged adequate and no system leaks were found. However, when a (111)-oriented Ge substrate was included along with the (100)-oriented Ge substrate in one of the experiments, the resulting Ge layer on the (111) substrate was relatively smooth and highly reflective, and for a measured concentration of 4×10^{19} cm^{-3} exhibited a hole mobility of 685 cm^2/V-sec.

over twice as high as any obtained in similarly doped p-type layers at any time earlier in the program.

It thus appeared that the pyrolysis process used for growing p-n junction structures in Ge by CVD was capable of producing material with properties adequate for solar cells. However, even at deposition temperatures as low as 650°C thermal type conversion of the 8-10 ohm-cm substrates was found to occur occasionally, depending primarily on the length of the deposition experiment. It was also found that Ge deposition in this lower temperature range often resulted in layers that were quite mottled in appearance for growth on both (100)Ge and (100)GaAs substrates, as if some contaminant had remained on the substrate surface prior to the deposition and despite the careful cleaning procedures used. Reducing the deposition rate (to ~500 Å/min) by decreasing the reactant concentrations improved the general appearance and the surface morphology of the film to some extent.

The photovoltaic performance of some of the Ge solar cell structures made by these CVD techniques was evaluated. The cell structures were grown on n-type single-crystal substrates of (100)Ge:Sb and (100)GaAs:Te. The p-type Ge layers were B-doped (from B_2H_6) and typically 1-5 μm thick; the n-type layers were undoped and typically ~7 μm thick. This group of structures had been grown at ~680°C by GeH_4 pyrolysis in H_2.

The composite wafers were processed either into 50 mil x 50 mil mesa diodes, with 25 mil x 25 mil top contacts, or into the conventional arrays of 0.5 cm x 0.5 cm individual cells using the standard solar cell contact pattern previously described. In-Au was used for the p-type contacts and Sb-Au-Ni for the n-type contacts.

The dark and illuminated I-V curves of a typical 50 mil x 50 mil Ge mesa diode grown on a GaAs substrate are shown in Figure 43. Under the illumination of the microscope lamp the I-V curve shifted as shown, and the I_{sc} is ~20 μA. The p-type Ge layer of this sample was ~5 μm thick.

The I-V curves for one of the 0.5 cm x 0.5 cm Ge cells grown on a Ge substrate are shown in Figure 44. This cell structure had a B-doped p-type Ge layer 1 μm thick on the n-type Ge substrate. The Ge deposition rate for this sample was slower than that of the structure represented in Figure 43. Large leakage currents are evident in both cells.

Fortunately, n-type Ge substrates of much lower resistivity (~0.03 ohm-cm) became available at that time and they were then used for the subsequent Ge deposition experiments. This allowed deposition temperatures of up to ~750°C to be used and this change immediately led to the growth of clean, smooth and highly reflective Ge films on both Ge and GaAs substrates. Measured electron mobilities (van der Pauw method) in the films also increased, from ~300 cm^2/V-sec for undoped n-type films grown at 650°C to ~400 cm^2/V-sec for films grown at 750°C (electron concentration ~3 x 10^{18} cm^{-3} in each case).

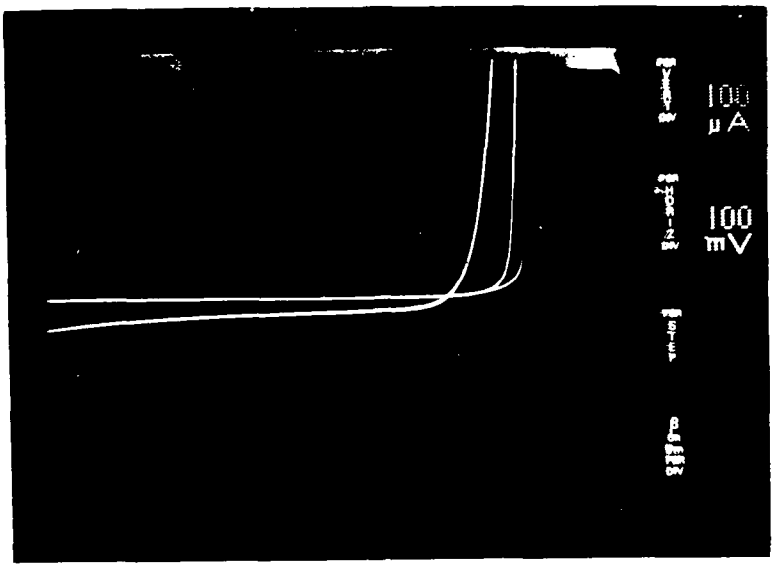


Figure 13. Dark and Illuminated (microscope lamp) I-V Curves for Ge p-n Junction Mesa-type Solar Cell Grown by CVD at ~ 680°C on GaAs:Fe Substrate (Cell 50 mil x 50 mil)

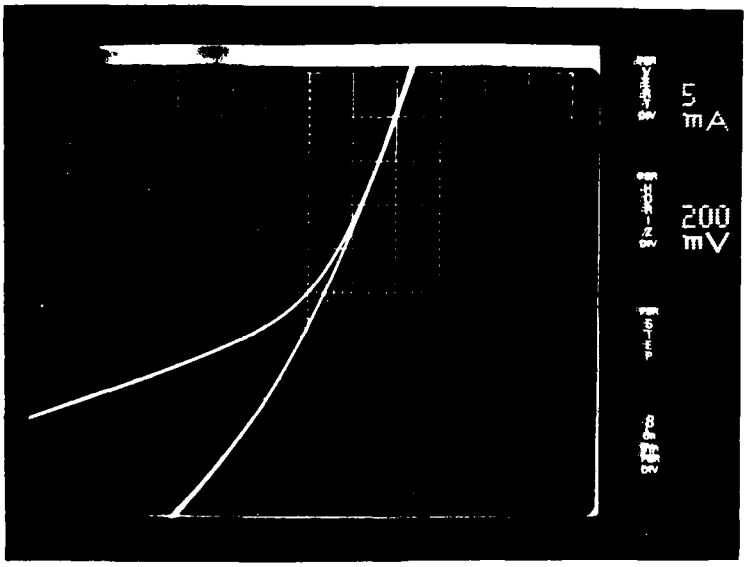


Figure 14. Dark and Illuminated (microscope lamp) I-V Curves for Ge p-n Junction Solar Cell (0.5 cm x 0.5 cm) Grown by CVD at ~ 680°C on Ge:Sb Substrate

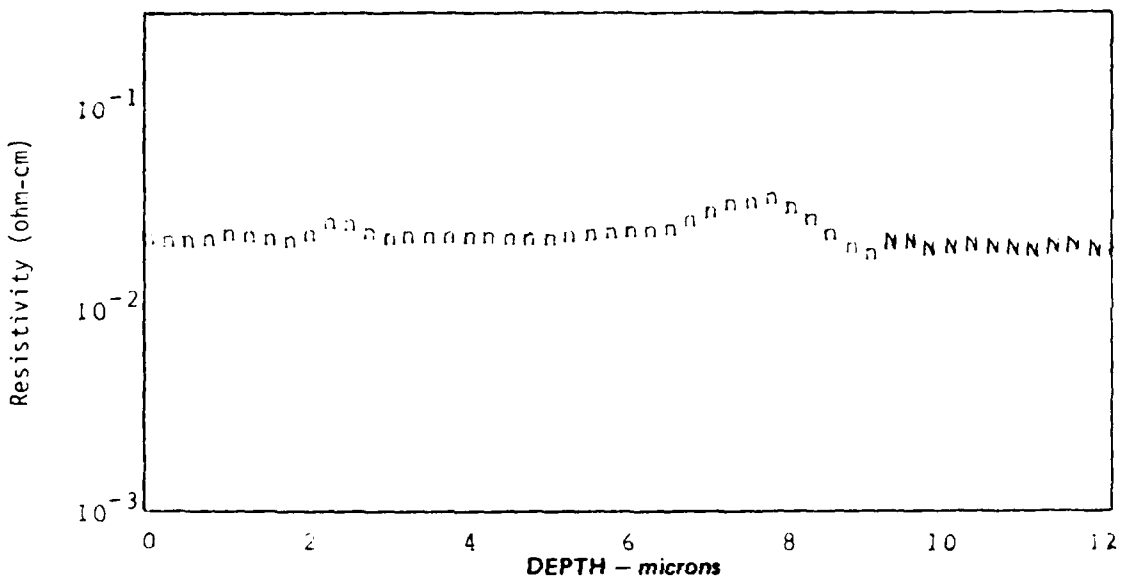
The success in achieving smooth and reflective Ge CVD layers by growth at higher temperatures (≥750°C) led to efforts devoted to obtaining increased layer growth rates and suitable impurity concentrations at the higher deposition temperatures, along with the improved surface morphology that results in that temperature range. The latter is important because of the need for subsequent growth of GaAs layers and/or the requirements of device processing and contacting.

Undoped CVD Ge films grown on Ge substrates at ~750°C at rates of 400-500 Å/min were found by spreading resistance measurements to be n type, with resistivities typically in the range 0.01-0.1 ohm-cm. However, similar films deposited on GaAs single-crystal substrates generally were p type, with resistivities typically ranging downward from 0.1 ohm-cm, the value depending upon the length of the deposition run. Spreading resistance data for two of these undoped Ge films grown in separate experiments on n-type (100)Ge:Sb substrates at ~750°C are shown in Figure 45.

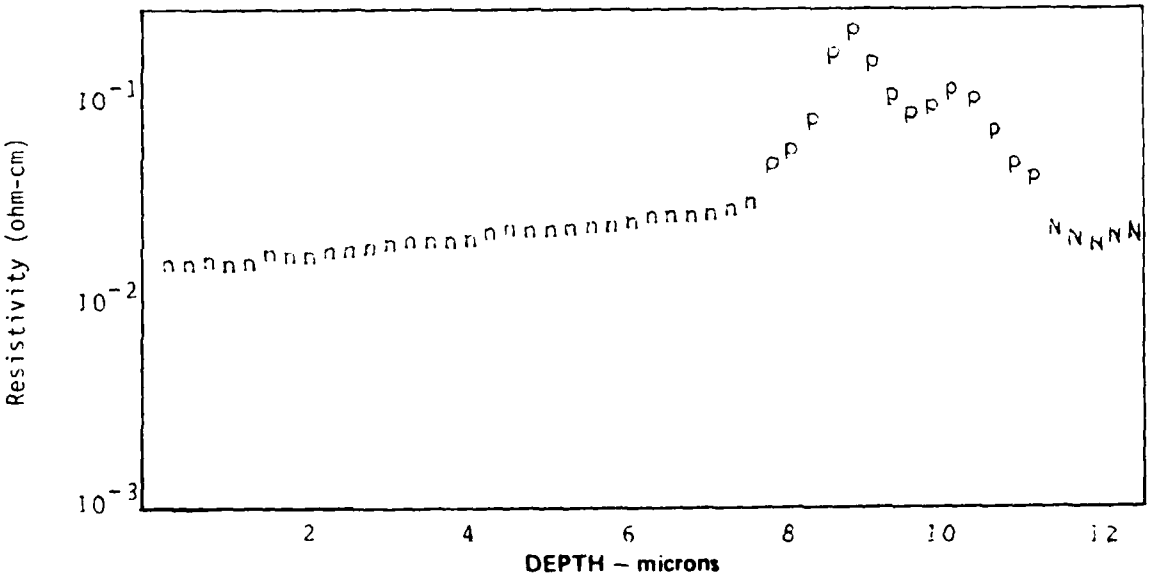
The Ge film grown in a 60 min deposition experiment at 750°C (Figure 45a) showed a uniform n-type resistivity of ~0.02 ohm-cm as a function of depth into the film except for a narrow region of slightly higher resistivity near the initial growth interface. The film grown at ~760°C in a 230 min deposition run (Figure 45b) was also n type over most of its thickness, with a resistivity of 0.02-0.03 ohm-cm in that range. However, in a region about 3 μm thick adjoining the growth interface the film was p type, as shown in the figure. The Ge film grown on semi-insulating (100)-oriented GaAs simultaneously with the film of Figure 45a was p type throughout the upper half of its thickness, but in a 3-4 μm region nearest the GaAs substrate it was alternately n and p type. The Ge film grown on GaAs simultaneously with the film of Figure 45b was p type throughout its thickness, although of rather erratically varying resistivity.

These results were interpreted in terms of an acceptor impurity entering the Ge film during growth – presumably Ga available in excess at the surface of the GaAs substrate due to As loss while the substrate was maintained at the relatively high deposition temperature. Relatively thick (i.e., ≥10 μm) Ge films grown under the above conditions (~750°C, ~400 Å/min growth rate), although fairly smooth and reflective in overall appearance, were found by SEM examination to contain sparsely distributed large rectangular pits typically 10 μm x 30 μm in size. Energy-dispersive x-ray analysis in the SEM established that these pits contained large concentrations of Ga metal, tending to confirm the above speculation about doping of the Ge films. A Ge film of comparable thickness deposited on GaAs at a lower temperature (650°C) to reduce the formation of free Ga at the growth interface did result in an n-type Ge film, but the surface was so strongly faceted crystallographically that it was judged unsatisfactory for device processing.

Attempts were then made to increase the Ge deposition rate significantly to minimize the Ga doping effect for growth on GaAs substrates. Undoped films were deposited at rates from 1500 to 3000 Å/min, and these were indeed found to be n type throughout. However, the surfaces were again very strongly faceted, with some facets having lateral dimensions of 4-6 μm. These results pointed out the difficulty in achieving simultaneously the desired conductivity type, resistivity, and



(a)



(b)

Figure 45. Spreading Resistance Data for Undoped Ge Films Grown by CVD on Single-crystal Substrates of n-type (100)Ge:Sb in Two Separate Deposition Experiments, Showing Effects of Possible Ga Doping of Ge Films; a) Deposition Temperature 750°C, Deposition Time 60 min; b) Deposition Temperature ~760°C, Deposition Time 230 min

surface morphology in Ge films deposited on GaAs substrates. Good epitaxial growth and good surface morphology are best obtained at higher deposition temperatures, while As loss from the substrate (with the attendant liberation of Ga) is minimized at lower temperatures. It is probable that further investigations at lower Ge deposition temperatures will be required to establish suitable growth conditions if the two-cell SMBSC is to be prepared by CVD growth on a GaAs substrate.

Most of the Ge CVD work thus continued to involve Ge substrates. Several deposition experiments were carried out at 800°C, at which temperature very good quality epitaxial growth is expected for the GeH_4 process. The anticipated improvements in film perfection and surface smoothness were obtained. Further, more efficient incorporation of B dopant (from B_2H_6) is realized at 800°C than at lower temperatures, for a given concentration (i.e., flow rate) of the dopant gas. Unfortunately, however, some disadvantages also accrue. In particular, evidence was found that Sb from the 0.02-0.03 ohm-cm n-type Ge substrate diffused into the growing Ge film at 800°C, resulting in a graded net impurity concentration profile in the doped p-type film in the region nearest the Ge substrate.

Figure 46 shows the spreading resistance scan obtained on one such sample, in which the B-doped Ge film was deposited at 800°C onto an n-type Ge:Sb substrate

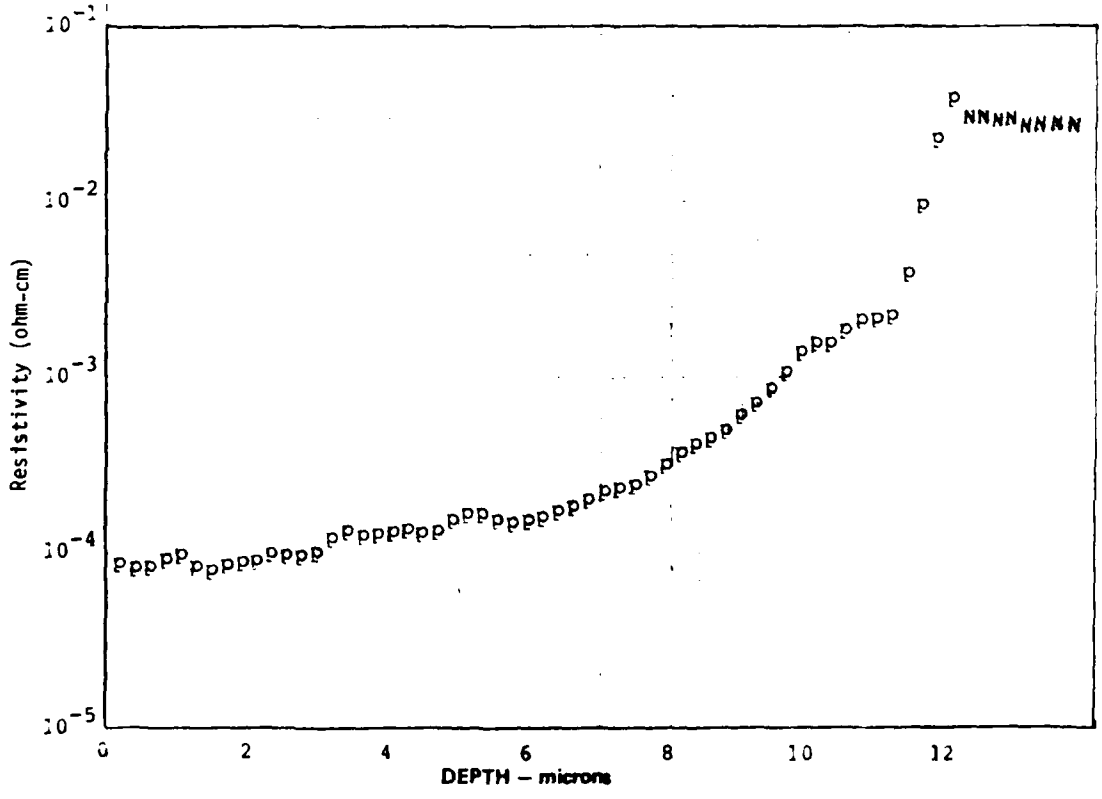


Figure 46. Spreading Resistance Data (as function of depth) for B-doped p-type Ge Film Grown by CVD at 800°C on Substrate of Single-crystal n-type (0.02-0.03 ohm-cm) Ge:Sb

in a run that continued for 4-1/2 hr (growth rate ~480 Å/min). The gradual increase in resistivity of the p-type film from a depth of ~3 μm below the surface to the initial growth interface at a depth of ~12 μm is consistent with a uniform vapor-grown B concentration profile and a typical diffused Sb profile compensating it from the interface outward. Fortunately, significantly higher deposition rates can be obtained at 800°C so that it is possible to obtain a doped Ge film of adequate thickness in several minutes of growth time, thus reducing the severity of the Sb out-diffusion problem.

Since the most likely configuration for the two-cell GaAs-Ge SMBSC involves a pGe/nGe CVD structure on an n-type single-crystal Ge substrate (see Section 2.2.5), most of the Ge CVD experiments in the remainder of Phase 1 involved that configuration. Furthermore, because of the good surface morphology obtained for growth at 800°C, that was the temperature consistently employed. Typical deposition rates ranging up to 0.7 μm/min were obtained, thus permitting growth of a 1-2 μm p-type (B-doped) Ge layer in 1.4 to 2.9 min, a time sufficiently short to keep Sb out-diffusion at an acceptable level. Although various cell processing difficulties related to contact definition continued with these Ge structures, numerous samples grown at 800°C at the higher growth rates were processed into 0.5 cm x 0.5 cm cells, and encouraging results were achieved. Typical structures involved p-type B-doped Ge CVD layers on n-type (0.02-0.03 ohm-cm) single-crystal (100)-oriented Ge substrates. Microscope lamp illumination and mechanical probe contacts were used for rapid screening of the cells.

The I-V curves obtained for one such cell structure are shown in Figure 47. This cell consisted of a p-type B-doped layer ($p \approx 4 \times 10^{18}$ cm^{-3}) ~2.5 μm thick grown at a deposition rate of ~1900 Å/min at 800°C on the n-type Ge:Sb substrate. Although very high series resistance and junction leakage are much in evidence for this cell, the observed open-circuit voltage V_{OC} of 200 mV and the short-circuit current density J_{SC} of ~35 mA/cm^2 are much improved over the corresponding parameters obtained for previous Ge cells made by CVD but at much lower deposition rates and lower growth temperatures. (Cf Figure 44.) This encouraging result provided the impetus for further development of this CVD procedure for making Ge cells for the SMBSC and for pursuing the specific two-cell structure discussed in Section 2.2.5.

To this end a new ultrahigh-purity GeH_4 source tank was obtained from Ideal Gas Products, Inc. (Edison, NJ), late in Phase 1 and was used in the preparation of a number of p/n Ge film structures on single-crystal Ge substrates. The GeH_4 was described by the manufacturer as the highest purity available and was obtained in 5 percent concentration in H_2. After a preliminary checkout run, a series of experiments was done in which Ge cell structures consisting of ~2 μm p-type (B-doped) layers on ~10 μm n-type (undoped) layers were grown on low-resistivity (~0.02-0.03 ohm-cm) n-type single-crystal (100)Ge substrates. All of the layers were grown at ~800°C at growth rates or either ~0.7 or ~0.13 μm/min, the rate determined by the concentration (i.e., flow rate) of GeH_4 in the H_2 carrier gas stream.

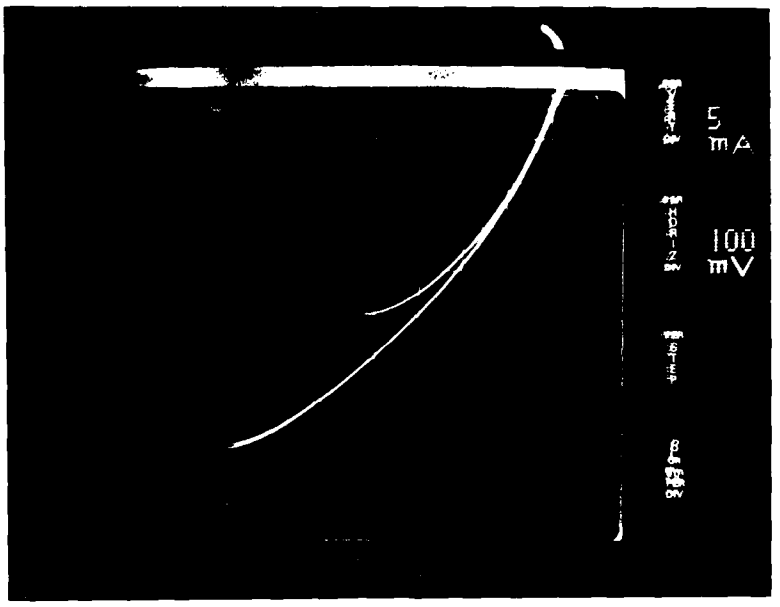


Figure 47. Dark and Illuminated (microscope lamp) I-V Curves for Ge p-n Junction Solar Cell (0.5 cm x 0.5 cm) Formed by p-type B-doped Ge Deposition (CVD) on n-type Ge:Sb (0.03 ohm-cm) Substrate at 800°C at Rate of ~1900 Å/min

The undoped n-type base layers of these cell structures typically exhibited a continuous gradation in electron concentration (actually in resistivity, as measured by a spreading resistance probe scan as a function of depth into the layer). The values ranged from ~1 x 10^{17} cm^{-3} at the film-substrate interface (corresponding to the substrate resistivity of 0.03 ohm-cm) to ~2.5 x 10^{16} cm^{-3} (~0.1 ohm-cm) at ~7 μm from the interface and ~5-6 x 10^{15} cm^{-3} (0.3-0.4 ohm-cm) at ~10 μm from the substrate surface. It thus appeared that the background (donor) doping concentration of the Ge CVD system with the new source was something less than 5 x 10^{15} cm^{-3} for growth at ~800°C. The results also indicated that Sb diffusion from the substrate into the undoped Ge CVD layer was still occurring during the growth process despite the relatively high deposition rates employed, and thus strongly influenced the properties of the n-type layers. Unfortunately, this apparent gradation in base-layer impurity distribution was not in the proper configuration for field-enhanced carrier collection when the structure was operated as a solar cell.

The 2 μm p layers were grown with a range of a factor of 25 in the diborane (B_2H_6) concentrations added to the GeH_4-in-H_2 gas stream. However, the corresponding measured hole concentrations in the top layers were found to vary by a factor of less than 10, indicating a sublinear relationship between acceptor dopant addition and effective carrier concentration (active impurity concentration) in this

operating range. Spreading resistance scans on several of the structures indicated that the 2 μm p layers had regions probably about 0.5 μm thick at the junction in which there was significant reduction in the net hole (and thus the net B impurity) concentration. This could have been the result of continued diffusion of the Sb (or other unidentified donor) from the n layer and substrate, although the observed effect might also have been an artifact of the method of measurement related to probe size and the various corrections involved in the spreading resistance technique.

Several of the Ge cell structures were processed into 1.6 mm x 1.6 mm mesa-type cell arrays at Thousand Oaks, using nominally the same processing sequence as was used earlier in preparing 0.5 cm x 0.5 cm Ge solar cells at Anaheim. These cells, along with several others processed at the same time in samples that had been grown earlier using the original (lower purity) GeH_4 source material, were characterized by dark and illuminated I-V measurements and spectral photoresponse measurements. Table 4 lists the principal deposition parameters, materials properties, and device characteristics of a number of these cells.

The principal distinction between these small-mesa cells and those fabricated earlier in the 0.5 cm x 0.5 cm size is that the smaller cells were characterized with unalloyed contacts. Due to unidentified difficulties in the contact alloying procedure, the alloying resulted in severely degraded cell performance whereas, of course, just the opposite effect should occur. The problem is illustrated for Ge cell samples 73 and 79 in the table, where measurements are given for both unalloyed and alloyed contacts. In both cases significantly lower V_{OC}, J_{SC}, and fill factor values were found after the alloying procedure, which consisted of heating the sample at 400°C in H_2 for 2 min.

In general, the V_{OC} values obtained for simulated AM0 illumination with these cells were lower than desired; open-circuit voltages of 250 mV or more should be achievable with Ge cells having good junction characteristics. However, as the above discussion of Ge layer growth indicates, the junction properties were known to be less than optimum in these structures – including those in which the active junction was formed at the interface between a deposited p layer and an n-type substrate wafer. The largest V_{OC} value observed for these cells – about 190 mV – should probably be viewed as acceptable for the junction quality represented. It seems certain that modifications could be readily introduced into the layer growth procedure to improve this parameter.

The maximum possible light-generated short-circuit current density that could be expected for Ge under AM0 illumination, with no reflection losses and 100 percent collection efficiency, is in the neighborhood of 75 mA/cm^2. (The corresponding value for Si cells is ~55 mA/cm^2.) Short-circuit current densities as high as 33 mA/cm^2 were obtained with these Ge cells, about 44 percent of the theoretical maximum. This is almost the same fraction of the maximum possible photogenerated current density as that often seen in production-model Si solar cells that are not optimized for maximum short-wavelength performance, and thus appears relatively good. In fact, most of the tabulated J_{SC} values exceed 25 mA/cm^2, a reasonable J_{SC} in view of the deficient infrared output of the ELH lamps used in the

Table 4. Principal Deposition Parameters, Materials Properties, and AM0 (no AR coating) Photovoltaic Performance Parameters of CVD Ge p/n Solar Cell Structures* Grown on Ge Substrates**

Sample No.	Depos. Temp. (°C)	No. of Grown Layers	Growth Rate (μm/min)	p Layer Thickness (μm)	Hole Concentr. (cm^{-3})	Hole Mobility (cm^2/V-sec)	n Layer Thickness (μm)	n Region Resistivity (ohm-cm)	Electron Concentr.† (cm^{-3})	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor	Effic. (%)
73-11	800	1	0.47	4.7	$1.8x10^{19}$	201	Note No. 1	0.025	$1.7x10^{17}$	191	16.1	0.64	1.5
73-11††	800	1	0.47	4.7	$1.8x10^{19}$	201	Note No. 1	0.025	$1.7x10^{17}$	147	13.9	0.56	0.85
75-7	800	1	0.12	2.5	$3.9x10^{18}$	354	Note No. 1	~0.03	$\sim 1x10^{17}$	189	32.3	0.60	2.7
77-5	800	2	p:0.12 n:0.09	1.8	$1.6x10^{18}$	130	7.0	0.10-0.03	$2.5x10^{16}$ $-1.3x10^{17}$	129	30.3	0.52	1.5
78-7	795	2	p:0.13 n:0.15	2.0	$2.9x10^{18}$	319	11.0	0.25-0.03	$8.0x10^{15}$ $-1.3x10^{17}$	127	26.4	0.53	1.3
79-9	795	2	p:0.60 n:0.67	1.8	$4.6x10^{18}$	504	10.0	0.35-0.04	$5x10^{15}$ $-9x10^{16}$	129	27.5	0.52	1.4
79-9††	795	2	p:0.60 n:0.67	1.8	$4.6x10^{18}$	504	10.0	0.35-0.04	$5x10^{15}$ $-9x10^{16}$	111	14.9	0.47	0.58
80-8	800	2	p:0.70 n:0.67	2.1	$3.1x10^{18}$	299	10.0	0.80-0.04	$1.6x10^{15}$ $-9x10^{16}$	150	31.3	0.57	2.0
81-2	804	2	p:0.67 n:0.65	4.0	$3.9x10^{18}$	604	13.0	0.30-0.03	$6x10^{15}$ $-1.3x10^{17}$	165	33.0	0.57	2.3

Note No. 1: Cell consists of p-type CVD layer directly on n-type substrate wafer.

*All fabricated cells 1.6mm x 1.6mm mesas (area 0.025 cm^2) with unalloyed contacts, except as noted.
**Ge substrates all n-type (100)-oriented ~ 0.03 ohm-cm wafers ~ 15 mils thick.
†Electron concentration deduced from measured resistivity, using standard data for single-crystal Ge. First figure given is that at p-n junction; second figure is for film at substrate interface.
††Measured after contact alloying (2 min. in H_2 at 400°C).

AM0 simulator* and the lack of an AR coating on the Ge to reduce the large (~36 percent) reflection losses typical of this material.

The first two samples listed (73 and 75) were grown using the original lower-purity GeH_4 source tank, and consisted of B-doped p-type layers grown at ~800°C on n-type (100) Ge substrates of 0.03 ohm-cm resistivity. These cells exhibited the largest V_{oc} values and fill factors of the group; although one of them had a high J_{sc} (32 mA/cm^2) the other had the lowest J_{sc} of the group. There were differences in the growth rates and the hole mobilities of the p layers for these two samples, but there does not appear to be an obvious explanation for the greatly reduced J_{sc} for cell 73-11.

Illuminated (AM0 simulator) and dark I-V curves for the best cell (75-7) of the group are given in Figures 48 and 49, respectively. The illuminated I-V curve clearly shows the poor curve shape (fill factor = 0.60). The cell efficiency of 2.7 percent increases to about 4.2 percent if allowance is made for the reflection losses. Another piece of this same Ge structure (sample 75) was processed earlier

*ELH lamps (manufactured by General Electric) have built-in dichroic reflectors that absorb some of the long-wavelength radiation as a means of reducing heating effects during illumination.

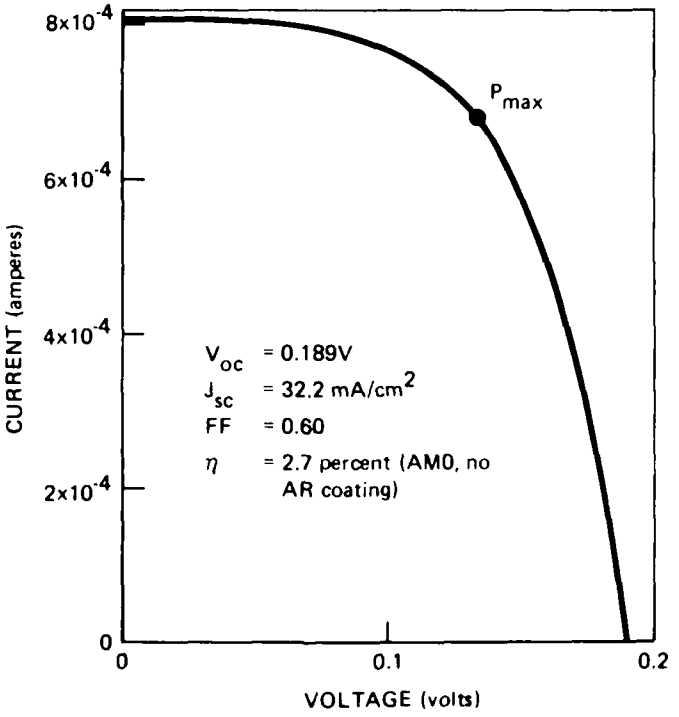


Figure 48. Fourth Quadrant of Illuminated (AM0 simulator) I-V Curve for Ge CVD Cell No. 75-7, Grown at ~800°C on (100)-oriented n-type 0.03 ohm-cm Ge Substrate Wafer (Cell size 1.6 mm x 1.6 mm)

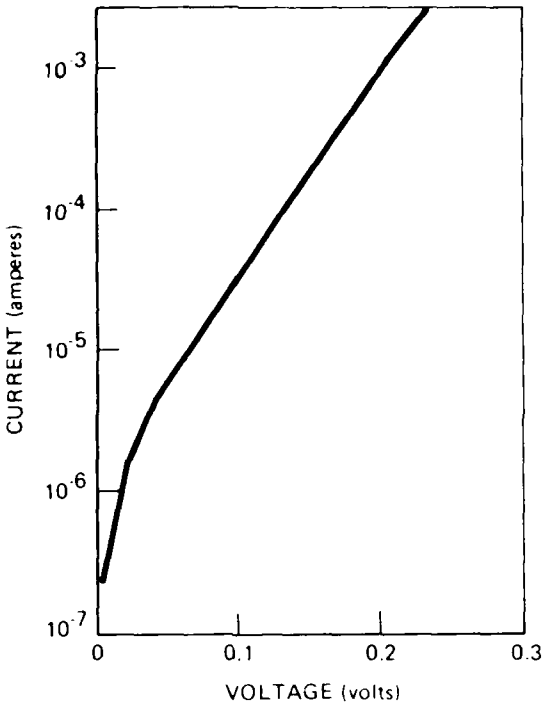


Figure 49. Dark Forward I-V Curve for Ge CVD Cell No. 75-7

in the program into 0.5 cm x 0.5 cm cells and characterized with microscope lamp (tungsten filament) illumination and mechanical probe contacts. The illuminated I-V curve so obtained for one of the cells in the array was shown in Figure 47 and exhibited a V_{OC} of ~200 mV and a J_{SC} of ~35 mA/cm^2 for that high-intensity illumination. Very high series resistance was indicated for that cell, with a fill factor much lower than that shown in the AM0 curve in Figure 48.

Figure 50 shows the measured spectral photoresponse curves for the best (75-7) and the poorest (73-11), as determined by J_{SC} values, of the cells listed in Table 4. The curve shapes are quite similar, particularly at the long-wavelength end ($\lambda > 1.2$ μm). The strong peak at ~1.54 μm and the weaker one at ~1.39 μm may be associated with the output spectrum of the tungsten lamp source in the spectrophotometer used for the measurements and with the fact that there had been no calibration of the apparatus in the wavelength range $\lambda >$ ~1 μm to assure uniform photon flux per unit spectral bandwidth. Also suspect is the fact that the response plummets at wavelengths significantly shorter than that of the Ge bandedge (~1.7-1.8 μm). Clearly, however, the major difference in the two cells in in the magnitude of the short-wavelength response and in the integrated areas under the curves, i.e., in the short-circuit current densities.

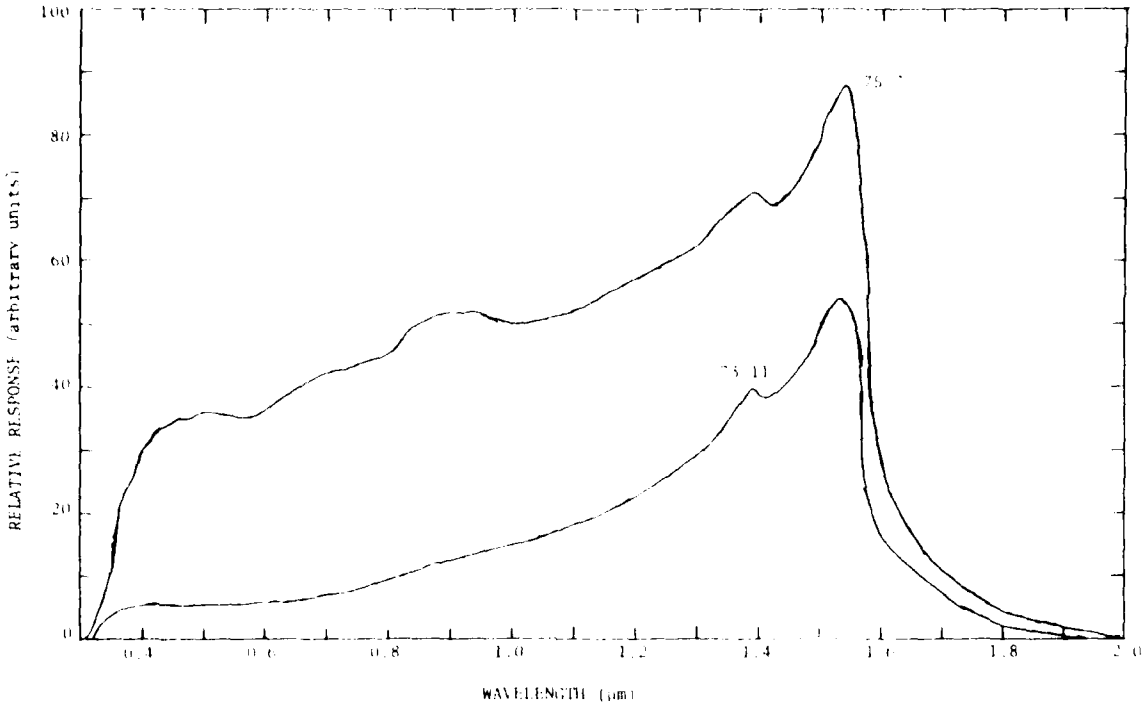


Figure 50. Relative Spectral Photoresponse of CVD Ge Solar Cells No. 75-7 and No. 73-11 (see Table 4) (Spectrophotometer uncorrected for $\lambda > \sim 1\mu m$)

Figure 51 shows the illuminated (AM0 simulator) I-V curves for cell 79-9 before and after alloying the contacts. This cell structure consisted of a 1.5 μm p layer on a 10 μm undoped n layer, both grown at a rate of 0.6-0.7 μm/min on an n-type Ge substrate. Before alloying, the cell had a V_{OC} value of 129 mV; after alloying it had decreased to 111 mV. The short-circuit current density, a respectable 27.5 mA/cm^2 before alloying, decreased drastically to 14.9 mA/cm^2 as a result of the alloying procedure. The fill factor, poor to start with, was only moderately affected by the alloying.

Another – and unexpected – result of the contact alloying procedure was the occurrence of a slow increase in the short-circuit current beginning immediately upon exposure to illumination. The rise time of the transient phenomenon was >10 sec. The extent of the effect is shown in Figure 52, which is a 20 sec time exposure of the illuminated I-V curve trace begun ~0.5 sec after the sample was initially exposed to the simulated AM0 illumination. Additional visual observation of the curve trace behavior during this transient period revealed that a steady state was reached in ~15 sec. This effect was noted for both samples (73-11 and 79-9) after alloying, but was not apparent with them or any of the other samples in the unalloyed condition. The phenomenon was tentatively attributed to the filling of very slow traps introduced in some way by the alloying process.

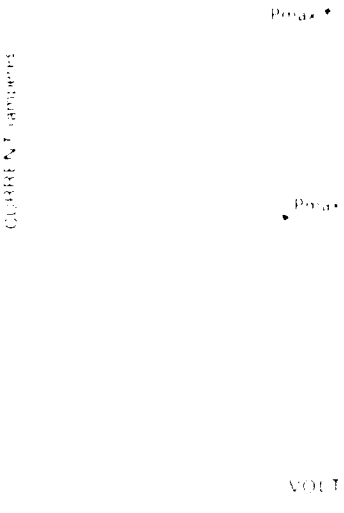


Figure 51. Fourth Quadrant of Illuminated (AM0 simulator) I-V Curves for CVD Ge Solar Cell No. 79-9 before and after Contact Alloying Procedure (2 min in H_2 at 400°C)

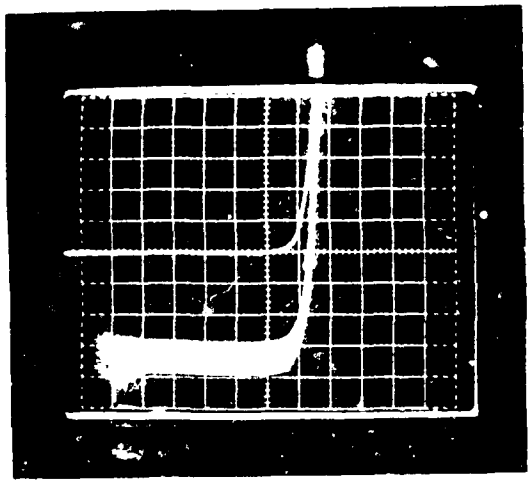
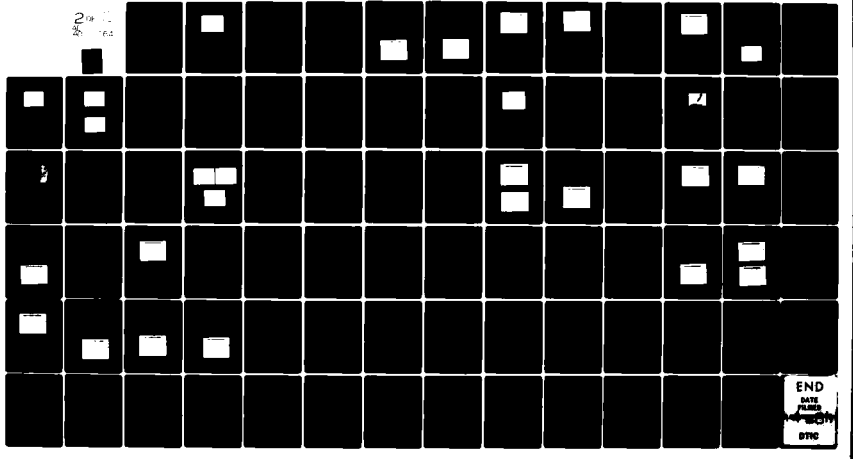
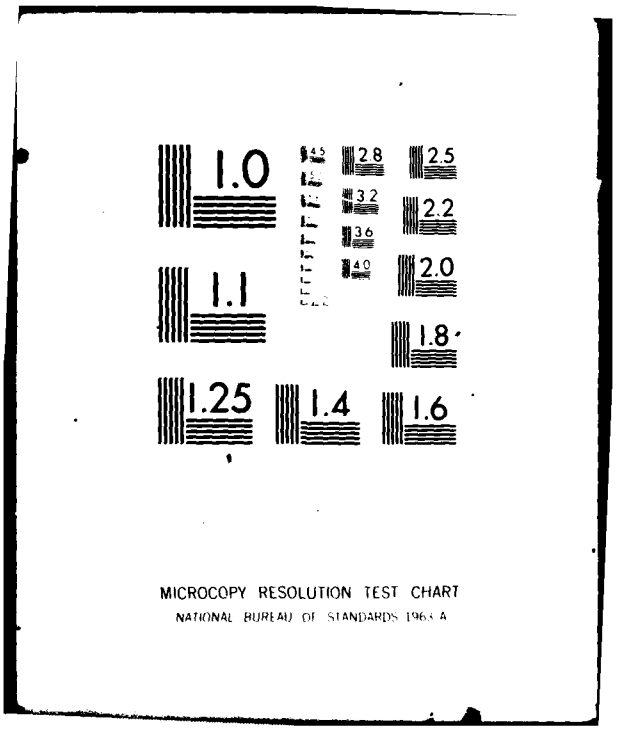


Figure 52. Dark and Illuminated (AM0 simulator) I-V Curves Obtained for CVD Ge Cell No. 73-11 (see Table I) after Contact Alloying Procedure, Showing Gradual Shift in Illuminated Curve over Period of ~15 sec following Exposure to Light

AD-A096 764 ROCKWELL INTERNATIONAL ANAHEIM CA ELECTRONICS RESEAR--ETC F/G 10/2
DEVELOPMENT OF HIGH-EFFICIENCY STACKED MULTIPLE-BANDGAP SOLAR C--ETC(U)
OCT 80 R P RUTH, J S HARRIS, P D DAPKUS F33615-78-C-2036
UNCLASSIFIED C78-1225.28/501 AFWAL-TR-80-2096 NL




1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

In summary, it can be stated that the results obtained with CVD growth of Ge solar cell structures improved markedly when the deposition work was transferred from a GaAs MO-CVD reactor system to a system that had previously been used only for Si CVD, and again when low-resistivity n-type Ge substrates became available so that higher deposition temperatures (up to 800°C) could be used. The accompanying use of increased deposition rates (up to 0.7μm/min) allowed sufficiently short growth times that the problem of Sb out-diffusion from the substrates was significantly reduced, but it is clear that intentionally doped n-type layers – rather than the nominally undoped n-type layers used to date – must be employed to improve the photovoltaic properties of the CVD Ge cells. In addition, relatively minor changes in cell design parameters – in particular, layer dimensions and layer doping concentrations – should result in significant improvements in cell performance. Also, modifications in the cell contacting procedures (especially the contact alloying schedules) are required to allow maximum device performance to be achieved for any cell design employed. These improvements will be sought in the Phase 2 investigations of CVD Ge cell structures.

2.2.3.2 Ge Solar Cell Structures by MBE

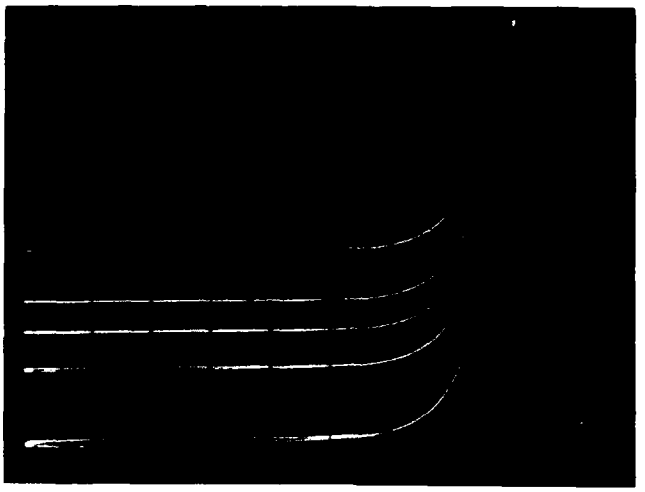
The first Ge solar cell structures made by the MBE process in this program were prepared near the end of Phase 1. One GaAs-Ge two-cell SMBSC configuration of potential interest involves n^+ layers deposited on p-type material, the opposite polarity of conventional window-type GaAs cells. This configuration is of interest because of the high diffusion rate of As compared with that of Ga in Ge, leading to the presence of an n^+ region in that portion of the Ge adjoining the GaAs-Ge interface. The resulting structure is a two-junction analog of the high-efficiency front-surface-field GaAs cell reported by Bozler et al (Ref 9).

As the first step toward fabrication of such a structure, As-diffused Ge solar cells were made by the MBE process and evaluated. A layer of As of suitable thickness was deposited on a p-type Ge substrate in the MBE system and subsequently held at elevated temperature to induce As diffusion into the (100)Ge substrate. Dark and illuminated I-V curves (at several intensities of illumination) for one such cell are shown in Figure 53, and a typical spectral photoresponse curve for another of these cells is shown in Figure 54.

This general procedure for preparing Ge cell structures by the MBE process was used further in the Phase 1 program in the fabrication of two-cell stacked structures of GaAs and Ge, as described in Section 2.2.5.

2.2.3.3 Ge Junction Structures by Thermal Diffusion

As indicated earlier, the possibility of preparing Ge junction structures for solar cell fabrication by means of conventional thermal diffusion of appropriate doping impurities into bulk (or thin-film) Ge was examined briefly in Phase 1 of this program. Although thermal diffusion is attractive from the point of view of low cost and scalability to large quantities of samples, diffusion of acceptor impurities into Ge is not a widespread contemporary technology.



Vert. scale:
20μA/div.

Horiz. scale:
50 mV/div.

Figure 53. Dark and Illuminated (microscope lamp) I-V Curves for Solar Cell (area 6.6×10^{-3} cm^2) Formed by Diffusing MBE-deposited As into p-type (100)Ge Substrate, Showing Effect of Variation of Incident Intensity

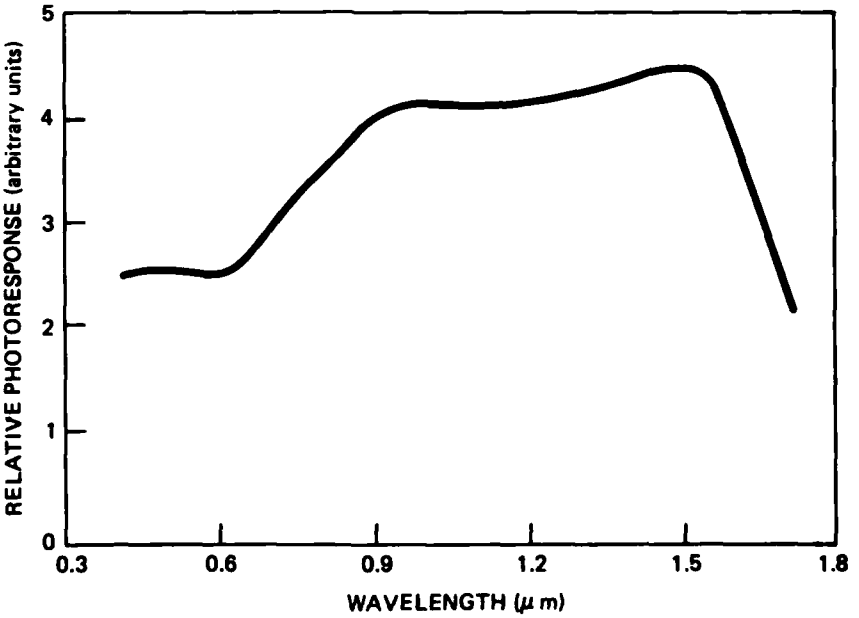


Figure 54. Relative Spectral Photoresponse for n/p Ge Solar Cell Made by MBE Deposition of As onto p-type (100)-oriented Ge Substrate Wafer Followed by Thermal Diffusion of the As

A relatively simple approach was proposed, involving the use of doped "spin-on" oxides – primarily SiO_2. Spin-on oxide sources were obtained (Emulsitone Corp.) with acceptor impurities of B and Ga for use in forming p-n junctions in n-type Ge wafers and/or films. The first attempts to achieve doping of Ge were not successful, however. The spin-on diffusion sources are designed primarily for use in doping Si and essentially no data was available from the manufacturer concerning their possible use with Ge. After some preliminary experiments with Si, several attempts were made to obtain boron diffusion from an oxide source into Ge bulk crystal material. The lack of success was attributed primarily to the fact that the boron diffusion coefficient in the oxide at temperatures usable with Ge (which melts at ~940°C) is too low to produce an acceptably high surface impurity concentration C_S at the Ge surface for satisfactory doping.

Consequently, a Ga spin-on diffusion source was tested. Calculations indicated a maximum possible C_S in this case would probably be in the range 5 - 9 x 10^{17} cm^{-3}. For a lightly doped n-type Ge substrate this might be sufficient for diffusion at ~850°C, but if less-than-optimum conditions prevailed then lower C_S values would be achieved and it might be impossible to produce a p-type region of acceptable properties.

The first experiments conducted with the Ga source were inconclusive. The only high-resistivity n-type Ge available at the time was the same 10 ohm-cm material that was used for the Ge CVD experiments described earlier, and thermal conversion of this material made it impossible to delineate a diffused junction anywhere below the surface by the usual staining or probing techniques. When relatively heavily doped (low 10^{17} cm^{-3}) n-type Ge wafers were used, again no diffused p-type region could be delineated--presumably because insufficient Ga had entered the lattice from the spin-on source.

Subsequent experiments, however, produced the desired results. A single-crystal substrate of n-type high-resistivity Ge was first coated with the Ga-doped spin-on oxide (SiO_2). The coated wafer was then heated at 850°C for 5 hr in a He atmosphere to diffuse the Ga impurity into the Ge. The results obtained are shown in Figure 55, which shows spreading resistance data obtained on this sample. A well-defined p-n junction is found at a depth of 2.0 μm, with the uniform resistivity of the n-type substrate delineated at greater depths and a typical diffusion profile shown by the resistivity scan through the surface layer. An indicated surface impurity concentration of ~10^{20} cm^{-3} and junction depth of 2.0 μm are commensurate with a diffusion coefficient of ~5x10^{-12} cm^2/sec, values comparable with literature values for Ga diffusion in Ge.

2.2.4 Connecting Intercell Junction Structures for GaAs-Ge SMBSC's

Several approaches were undertaken to solve the problem of the required high-conductivity connecting junctions between cells of the various SMBSC configurations included in the Phase 1 program. For the GaAs-Ge two-cell SMBSC it would be possible to form such a junction in either the GaAs or the Ge, although the former is preferable to allow as much as possible of the low-energy solar radiation that penetrates the GaAs cell unabsorbed to generate potentially collectible charge pairs in the low-bandgap Ge cell. No attempts were made during the Phase 1 program to form low-resistance tunneling junctions in Ge, although that possibility may be examined in Phase 2 if it appears justified.

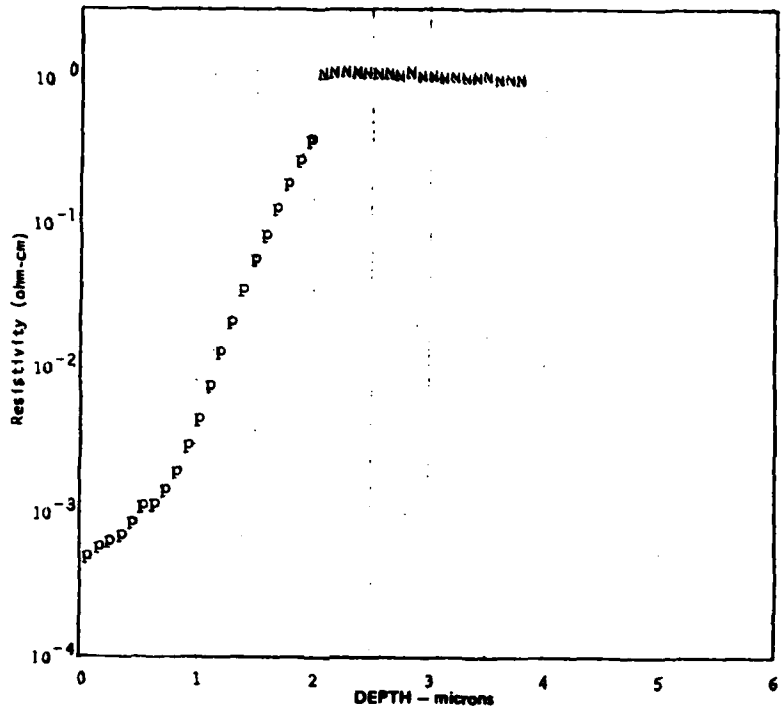


Figure 55. Spreading Resistance Data for n-type Ge Single-crystal Wafer with p-n Junction 2.0μm Deep Formed by Diffusion of Ga at 850°C for 5 hr in He, Using Spin-on Oxide Diffusion Source

The formation of conducting junctions in GaAs received considerable attention in the Phase 1 program, primarily by means of the MO-CVD technique but also by MBE methods. Although much of the work was done for the purpose of achieving connecting junctions between GaAlAs and GaAs cells (Tasks 4 and 5, Sections 2.4 and 2.5), all of the investigations of tunneling junctions in GaAs are described here.

2.2.4.1 GaAs Tunneling Junctions by MO-CVD

Early in the program a series of p^+/n^+ double-layer GaAs structures was grown by MO-CVD on both GaAs and Ge single-crystal substrates. These configurations were prepared for evaluation for possible use as the conducting tunnel junction between cells in the GaAs-Ge SMBSC. Zn and Se were used as the doping impurities for the p^+ and n^+ layers, respectively. Structures were grown at both 700 and 750°C. Small-area mesa devices were formed for evaluation.

The structures on GaAs substrates were grown at temperatures of 750, 700, 680, and 650°C; each consisted of a GaAs:Zn epitaxial p^+ layer grown on an n^+GaAs:Se layer that was grown on an n-type (100)-oriented GaAs:Si substrate. The wafers were processed into 25x25 mil mesa diodes using the Cr-Au contacts as etching masks. The diode I-V curves showed evidence of an increasing doping concentration at the junction for decreasing growth temperature. The structures grown at 650°C produced good tunnel diodes having I-V characteristics such as that shown in Figure 56.

One of the GaAs tunnel diode structures grown at 650°C was subsequently annealed at the same temperature for 30 min to simulate thermal conditions that would exist during MO-CVD growth of a GaAlAs/GaAs solar cell structure on the epitaxial GaAs tunnel diode. This structure was processed into 25 mil x 25 mil diodes and characterized. It was found that all of the devices exhibited "backward diode" rather than tunnel diode I-V characteristics. It was not known at the time if the subsequent elevated-temperature processing had caused the lack of tunneling behavior.

After rechecking proper deposition conditions for GaAs (as well as GaAlAs) film growth at 700°C, since the preliminary experiments had shown that GaAs tunnel diode structures should be deposited at temperatures lower than those normally used (i.e., ~750°C) for GaAs growth, additional tunnel junction structures were prepared. Shortly thereafter (in the eighth month of the program) the first GaAlAs-GaAs two-cell SMBSC structures (see Task 4, Section 2.4) were grown by MO-CVD, with the GaAlAs cell and the GaAs cell connected by an n^+-p^+ junction structure either in GaAlAs or in GaAs. An example of each was grown, although only the structure

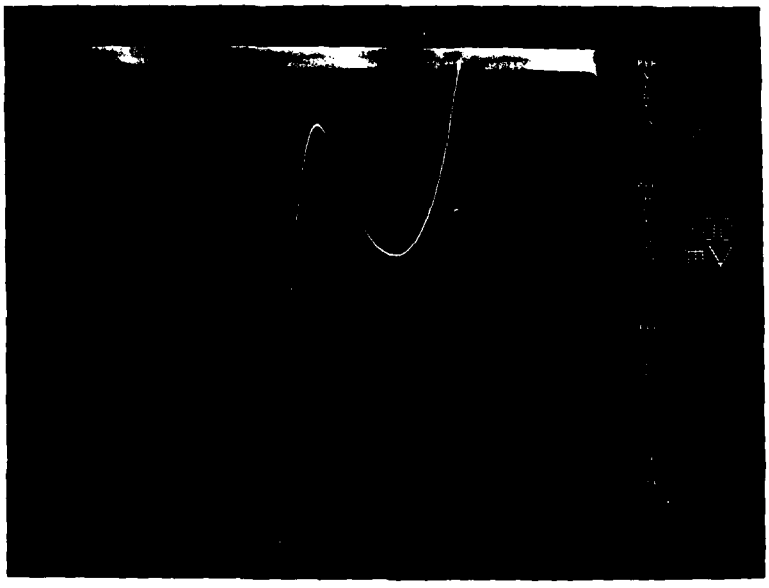


Figure 56. Tunneling I-V Characteristic for 25x25 mil Mesa Diode in p^+GaAs:Zn/n^+GaAs:Se Epitaxial Structure Grown by MO-CVD on nGaAs:Si Substrate at 650°C

with the connecting junction in the GaAs exhibited tunneling properties. Further discussion of the properties of those particular structures is given in Section 2.4.

A subsequent group of tunnel junction structures was prepared at lower deposition temperatures of 630 and 650°C, with n^+/p^+ structures consisting of GaAs:Se/GaAs:Zn and p^+/n^+ structures consisting of GaAs:Zn/GaAs:Se. The n^+/p^+ devices were grown at both 630 and 650°C, and the layers were each ~0.6 μm thick. The samples were processed into mesa diodes of the customary dimensions (0.050 in x 0.050 in) and had the usual 0.025 in x 0.25 in Cr-Au contacts on the n^+ top layer.

I-V characteristics of two representative n^+/p^+ devices deposited at ~650°C and ~630°C are shown in Figures 57 and 58, respectively. Diodes grown at 650°C showed a weak tunneling current component in the characteristic, as seen in Figure 57. However, those grown at ~630°C (Figure 58) exhibited almost a linear I-V curve, indicating that the doping concentrations on both sides of the junction were so high that tunneling occurred even at bias voltages near zero. It can be seen from Figure 58 that the device had a voltage drop of ~0.150V for a current density of ~3A/cm^2. This conductivity is more than adequate for a layer to be used as an intercell connection, so it appeared that the necessary parameters for joining the two cells in this SMBSC structure could indeed be achieved by growth at relatively low temperatures--an important requirement. The extent to which these tunneling structures would be consistently preserved during subsequent higher-temperature growth of GaAs and/or GaAlAs cells in a tandem stack, however, remained to be established.

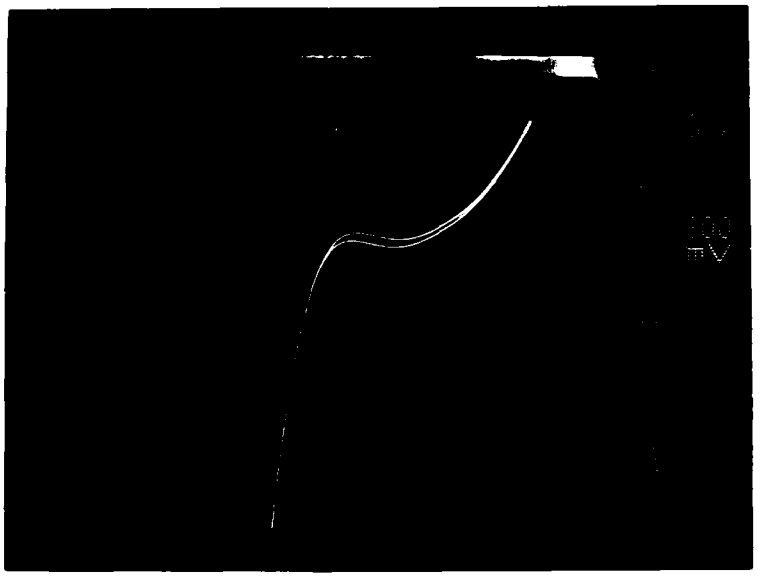


Figure 57. I-V Characteristic of GaAs:Se/GaAs:Zn n^+/p^+ Tunnel Junction Structure Grown by MO-CVD at ~650°C on GaAs Single-crystal Substrate (Mesa dimension 0.050 x 0.050 in)

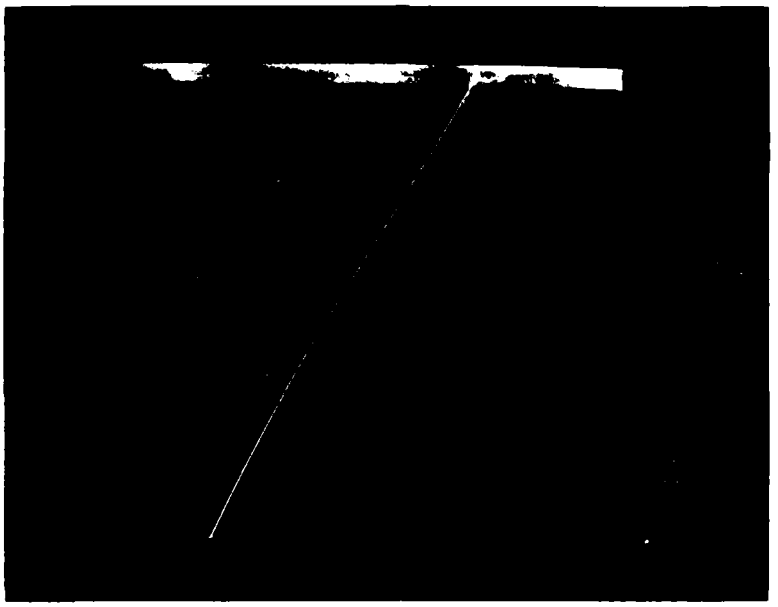


Figure 58. I-V Characteristic of GaAs:Se/GaAs:Zn n^+/p^+ Tunnel Junction Structure Grown by MO-CVD at ~630°C on GaAs Single-crystal Substrate (Mesa dimension 0.050 x 0.050 in)

A somewhat different n^+/p^+ GaAs tunnel structure was also grown at about the same time, this one involving an n^+ GaAs:Se layer deposited by MO-CVD at ~630°C on a p^+ GaAs:Be layer grown by MBE. The p^+ ($\sim 1 \times 10^{19}$ cm^{-3}) layer was ~1 μm thick and was deposited on a GaAs:Cr single-crystal substrate; the MO-CVD n^+ layer ($1\text{-}2 \times 10^{19} cm^{-3}$) was ~6.0 μm thick. Mesa diodes (0.050 in. x 0.050 in.) were fabricated in the sample by carefully etching down to the thin p^+ layer. Top contacts were the usual 0.025 in. x 0.025 in. square pads of Cr-Au. The p^+ Be-doped layer was also contacted by 0.025 in. x 0.025 in. pads of Cr-Au.

The I-V characteristic of a typical device on this sample is shown in Figure 59, and the dark log I-V curve for one of the devices on this sample is shown in Figure 60. There is a sufficient valley-current component from interface-state tunneling to convert the negative-resistance region to one of constant current independent of voltage in the range 0.1-0.2V. The I-V curve is not as good as that of the n^+/p^+ structure of Figure 58, which was also grown at ~630°C, but the results did demonstrate that useful tunnel structures could be prepared by the combination of MO-CVD and MBE processes and that the abrupt n^+/p^+ interface apparently remained after more than 30 min at the MO-CVD growth temperature. This property results from the low diffusivity of both Be and Se as impurities in GaAs and may be important to preserving good tunneling characteristics in structures during subsequent growth of the top cell in tandem cell assemblies.

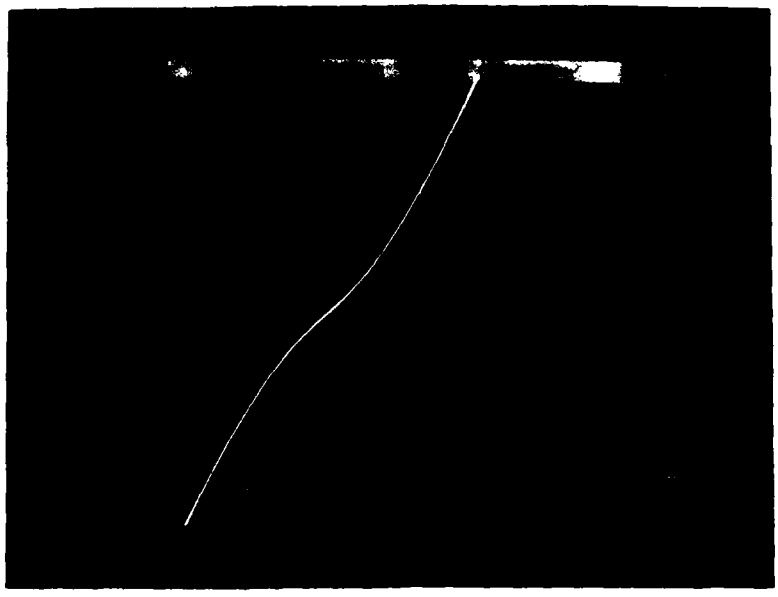


Figure 59. I-V Characteristic of n^+/p^+ GaAs:Se/GaAs:Be Hybrid Tunnel Structure Made by Growing MO-CVD Layer on Previously Grown MBE Layer on Single-crystal GaAs Substrate

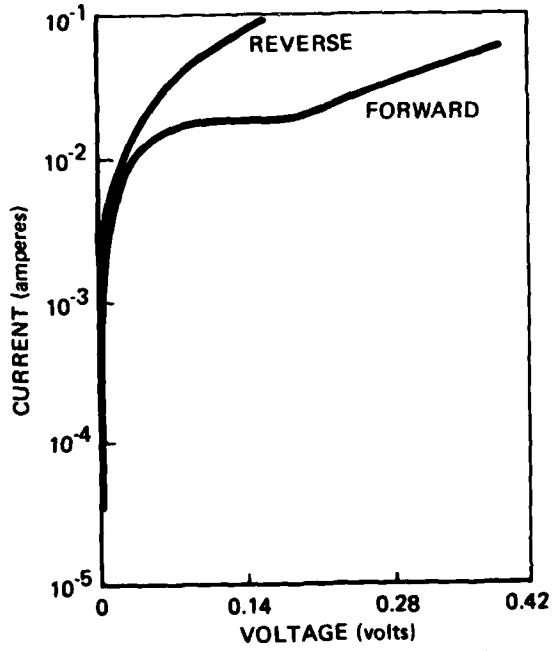


Figure 60. Dark Log I-V Curve for Hybrid MO-CVD/MBE n^+GaAs/p^+GaAs Tunnel Junction Structure on GaAs Substrate

Figure 61 shows the log I-V curve for a more heavily doped tunnel junction structure prepared entirely by MO-CVD. An n^+ GaAs layer (Se-doped, $\sim 2 \times 10^{19}$ cm^{-3}) was grown to a thickness of ~ 0.6 μm onto a p^+ GaAs layer (Zn-doped, $\sim 5 \times 10^{18}$ cm^{-3}) grown to a thickness of ~ 1.5 μm on a p-type Zn-doped ($\sim 10^{18}$ cm^{-3}) GaAs substrate. The I-V characteristic is seen to be essentially ohmic over the entire range examined. Such wide-range ohmic behavior is probably attributable to the heavy doping used in both layers.

A comparison of the slopes of the forward characteristics for equal-area mesas of the two structures of Figures 60 and 61 shows little difference for currents below about 4×10^{-3}A. For the mesa areas used (0.015 cm^2) this corresponds to a current density of ~ 0.27 A/cm^2, a level well above that attainable in a solar cell under 1-sun AM0 conditions. The contact resistance for these tunnel junctions was calculated to be < 0.023 ohm-cm^2 and appears to be nearly independent of doping level in the range of current densities of interest for 1-sun SMBSC applications.

An I-V characteristic typical of the p^+/n^+ GaAs:Zn/GaAs:Se tunnel diode structure grown at $\sim 630^oC$ is shown in Figure 62. As before, mesa diodes 0.050 in. x 0.050 in. were fabricated, with Cr-Au contacts to both regions. The electrical behavior observed in this structure was similar to that found for the n^+/p^+ MO-CVD structure grown at $\sim 650^oC$ (Figure 57) but superior to that obtained with a similar p^+/n^+ structure grown at $\sim 650^oC$.

Application of these GaAs tunneling junctions made by MO-CVD to the preparation of two-cell GaAlAs-GaAs SMBSC's is discussed in Sections 2.4.2 and 2.4.3.

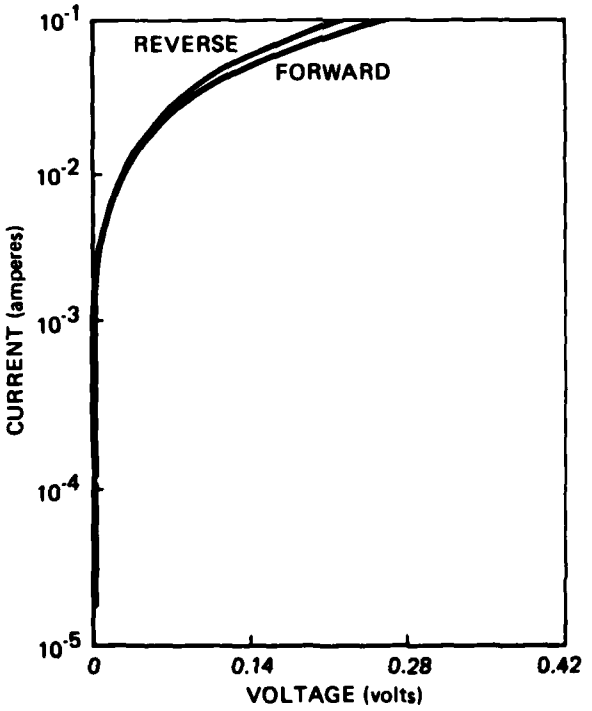


Figure 61. Dark Log I-V Curve for n^+GaAs/p^+GaAs Tunnel Junction Structure Grown Entirely by MO-CVD on GaAs Substrate

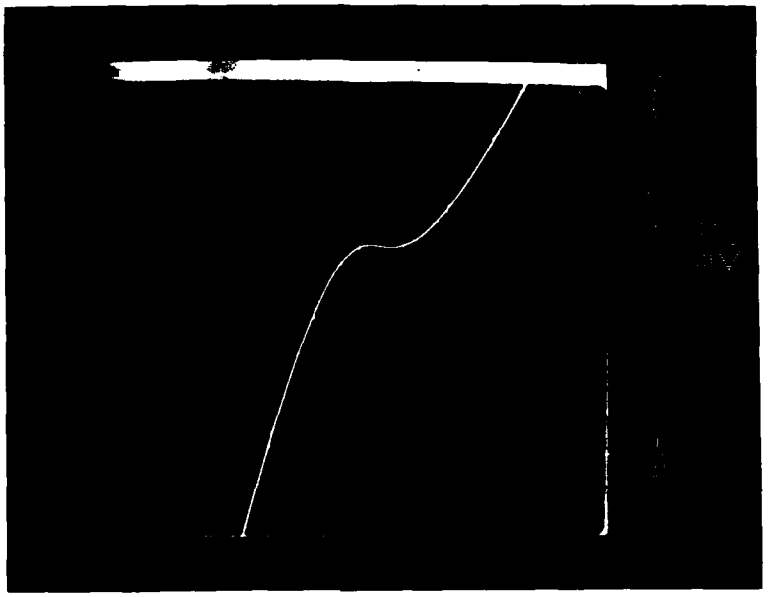


Figure 62. I-V Characteristic of p^+/n^+ GaAs:Zn/GaAs:Se Tunnel Diode Structure Grown by MO-CVD at ~630°C on Single-crystal GaAs Substrate

2.2.4.2 GaAs Tunneling Junctions by MBE

Some preliminary experiments on the formation of a conducting connecting junction for the GaAlAs-GaAs portion of the three-cell SMBSC structure to be developed in Task 5 by LPE techniques were carried out in the eighth month of the program. Molecular-beam epitaxy (MBE) techniques were used to deposit an n^+/p^{++} double layer of GaAs on a p^+ GaAs single-crystal substrate at a temperature of ~540°C. The layer structure that was formed is shown schematically in Figure 63.

The hole mobility in the p^{++} Be-doped layer was estimated to be ~35 cm^2/V-sec on the basis of measurements made on a separate layer grown under the same deposition and doping conditions. The contact resistivity obtained for the top contact was found to be 0.13 ohm-cm^2.

Figure 64 shows the forward- and reverse-current oscilloscope trace obtained with this n^+/p^{++} GaAs junction structure, illustrating its ohmic behavior but the lack of any indication of a true tunneling characteristic. The observed ohmic behavior may have been as much a consequence of a high structural defect concentration in the vicinity of the n^+/p^{++} interface as of the high intentional doping concentration in the two regions. In any case the ohmic behavior observed might be acceptable for the purpose.

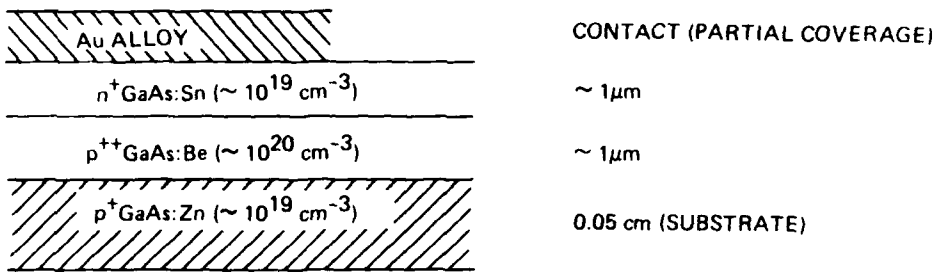


Figure 63. Configuration of n^+/p^{++} Conducting Junction Structure Formed by MBE on Single-crystal GaAs Substrate at 540°C

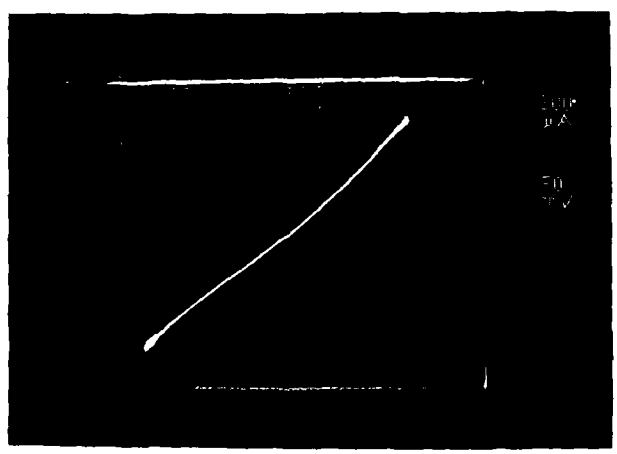


Figure 64. Typical Forward and Reverse Oscilloscope Trace Obtained with n^+/p^{++} GaAs Conducting Junction Structure Grown by MBE at ~540°C, on p^+GaAs:Zn Substrate, Showing Ohmic Behavior

A second MBE n^+/p^{++} structure was grown at about the same time, and consisted of thin (~500Å) layers of n^+ Sn-doped and p^{++} Be-doped GaAs sandwiched between lightly doped (10^{15}-10^{16} cm^{-3}) layers of n-type and p-type GaAs each ~1μm thick. The heavily doped region in this structure was considered to be a close analog of the structure believed suitable for forming the connecting intercell ohmic contacts in the LPE-grown GaAℓAs-GaAs cell pair being developed in the Task 5 work (see Section 2.5). It was found that this structure also exhibited ohmic (i.e., non-rectifying) behavior.

Both of the above structures were subjected to thermal cycling procedures that duplicated the temperature-time cycle typical of that involved in LPE growth of a window-type GaAs solar cell structure. Subsequent examination of the I-V characteristics of both structures indicated no deleterious effect on the ohmic conduction nature of either structure. The structural parameters and the electrical characteristics of these samples both before and after the temperature cycling are summarized in Table 5.

The I-V characteristics for the first sample after this temperature cycling are shown in Figure 65 and for the second sample before and after the cycling in Figure 66. The observed behavior of both structures after the heat treatment indicated that a satisfactory connecting junction that will survive subsequent processing can be made by the MBE technique.

Table 5. Structural Parameters and Electrical Properties of GaAs Nonrectifying Junction Structures Grown by MBE, before and after Temperature Cycling*

Sample Designation	Individual Layer Parameters				Measured Contact Resistivity	
	Cond. Type	Carrier Conc. (cm^{-3})	Dopant	Thickness (μm)	Before Temp. Cycling (ohm-cm^2)	After Temp. Cycling (ohm-cm^2)
236	n^+	10^{19}	Sn	1.5	0.13	0.196
	p^{++}	10^{20}	Be	1.8		
	p^+	10^{19}	Zn	(substrate)		
239	n	10^{16}	Sn	1	0.31	0.123
	n^+	2×10^{19}	Sn	0.05		
	p^+	5×10^{19}	Be	0.05		
	p	10^{16}	Be	1		
	p^+	10^{19}	Zn	(substrate)		

*Temperature cycling duplicated that associated with LPE growth of window-type solar cell structure in GaAℓAs-GaAs materials system.

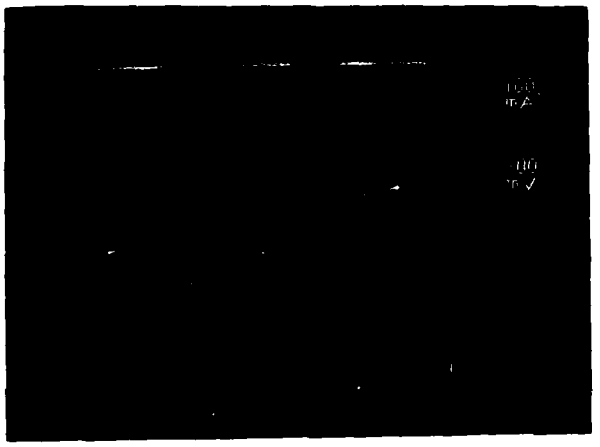


Figure 65. Forward and Reverse I-V Characteristics of n^+/p^{++} GaAs Conducting Junction Structure of Figure 64 Grown by MBE at ~540°C on p^+GaAs:Zn Substrate, after Temperature Cycling Duplicating that Encountered in LPE Cell Growth

2.2.4.3 Optical Properties of GaAs Tunneling Junctions

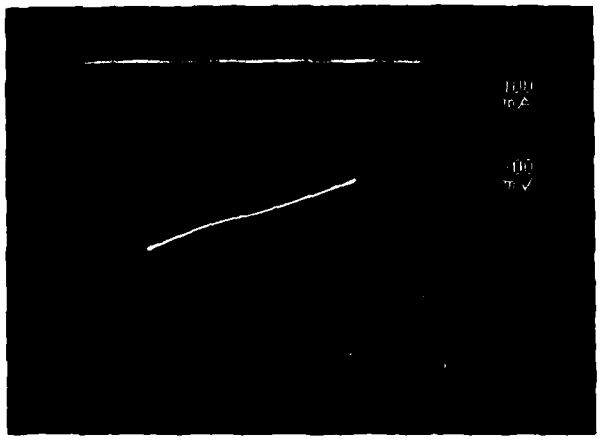
To assess the possible optical absorption losses associated with GaAs tunnel junctions, a review of the below-bandgap-energy absorption data for highly doped GaAs was made.

The data suggest that to maintain an attenuation of less than 1 percent of the 0.7eV photons by the tunnel junction the p^+ layer thickness can be no more than ~160Å for a doping concentration of 10^{20} cm^{-3} and the n^+ layer thickness no more than ~1300Å for 10^{20} cm^{-3}. For 10^{19} cm^{-3} doping concentrations in each region these limiting thicknesses increase to ~0.24μm for p^+ material and ~0.6μm for n^+ material.

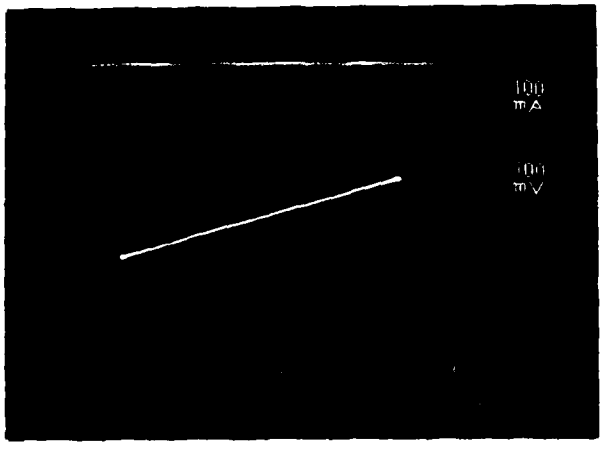
The latter parameters are within the range of those practically attainable with any of the fabrication techniques being considered for producing the stacked multi-junction structures in this program.

2.2.5 Experimental GaAs-Ge SMBSC Structures

A likely configuration for the first experimental two-cell GaAs-Ge SMBSC to be fabricated by CVD techniques is shown schematically in Figure 67. Although the separate components involved (GaAs cell, GaAs tunneling junction, Ge cell) were made separately in the Phase 1 program the entire stacked cell assembly had not been fabricated by CVD techniques alone prior to the completion of Phase 1.



(a)



(b)

Figure 66. Forward and Reverse I-V Characteristics of $n/n^+/p^+/p$ GaAs Conducting Junction Structure Grown by MBE on p^+GaAs:Zn Substrate (a) before and (b) after Temperature Cycling Duplicating that Encountered in LPE Cell Growth

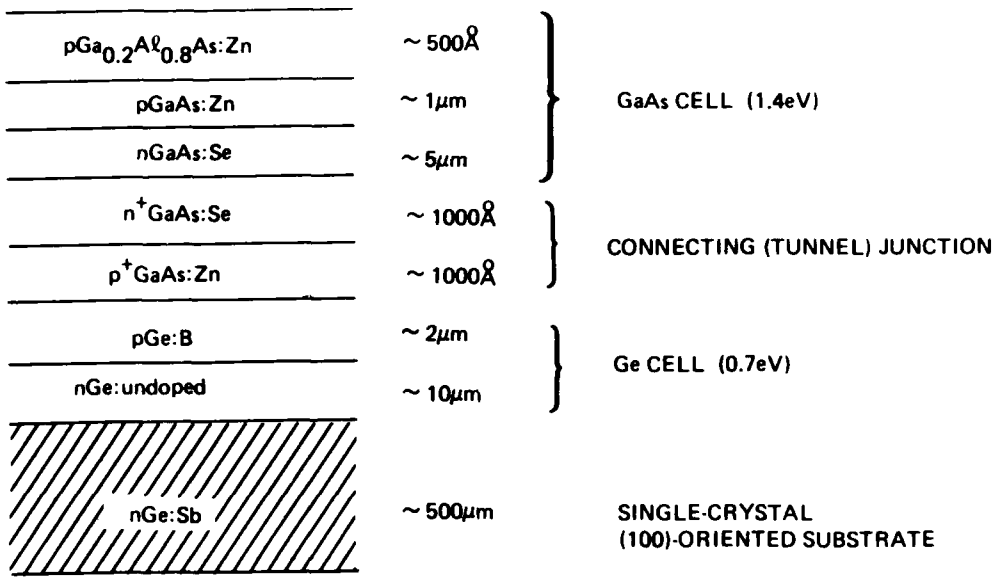


Figure 67. Probable Configuration of GaAs-Ge Two-cell SMBSC Made Entirely by CVD Techniques

However, near the end of the Phase 1 program considerable attention was given to the GaAs-Ge stacked cell using MBE techniques. The intended (i.e., grown) structure of one such experimental cell assembly was $p^+Ga_{0.2}Al_{0.8}As/pGaAs/nGaAs/n^+GaAs/p^+GaAs/nGe$(As-diffused)/pGe. The upper three layers formed the conventional window-cell structure, while the n^+GaAs/p^+GaAs region constituted the conducting tunnel junction. The Ge cell structure employed was that found feasible to fabricate by depositing As on a p-type Ge substrate and subsequently diffusing the As into the Ge to form an n/p Ge junction. The design was clearly not optimum because of the apparently opposing junctions of the upper and lower cells. However, for purposes of demonstrating the formation of a double-cell stack by MBE it appeared as the most expedient structure to use.

The structure did not exhibit a very large open-circuit voltage (<0.9V) but it did appear to consist of two additive – rather than opposing – junctions. Figure 68 shows the spectral response curve obtained for this device, with the longer wavelength response ($0.87\mu m < \lambda < 2.0\mu m$) corresponding to the Ge response. The shape of this part of the response, increasing gradually to about the wavelength of the GaAs band edge (~0.87μm), indicates that a GaAs-Ge heterojunction rather than a Ge homojunction was involved. The response in the region $0.35\mu m < \lambda < 0.87\mu m$ is due to GaAs. Since the peak of this response region is at the blue end (~0.4μm) and the response drops so abruptly for shorter wavelengths it appears that the actual GaAs cell structure achieved was not a heteroface structure as intended but rather a GaAlAs-GaAs heterojunction cell involving the $p^+Ga_{0.2}Al_{0.8}As$ window layer and

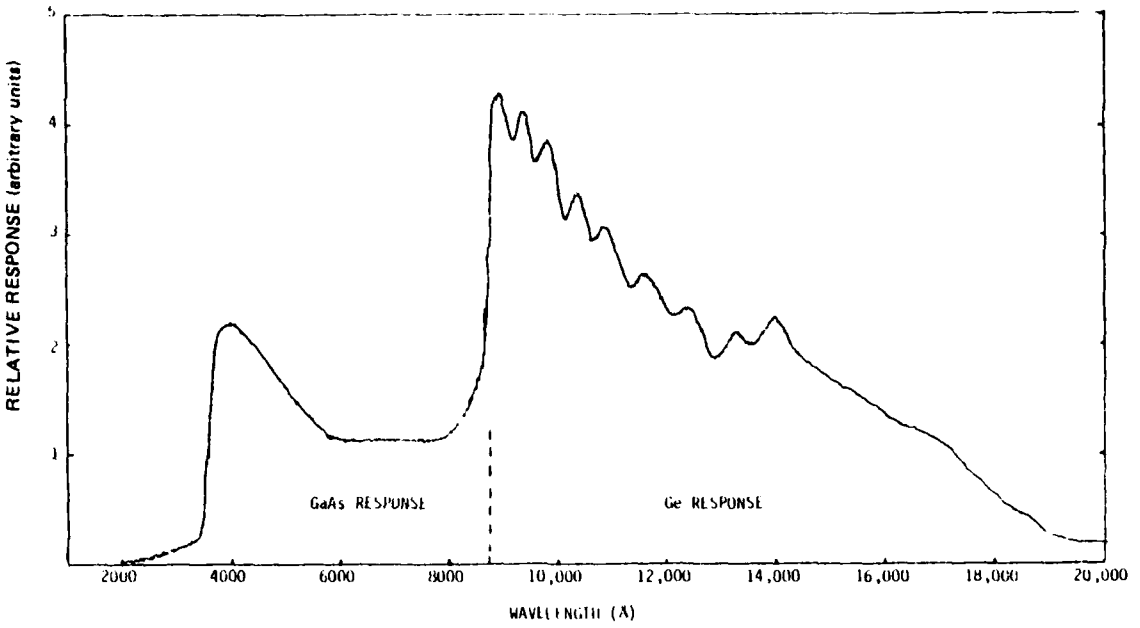


Figure 68. Spectral Response Curve for MBE-grown Stacked Two-cell Structure Having Apparent Configuration $p^+Ga_{0.2}Al_{0.8}As/nGaAs/n^+GaAs/p^+GaAs/nGe$

the nGaAs active layer, with the pGaAs layer somehow being excluded (or perhaps not successfully produced in the deposition). The existence of significant (in fact, peak) response at wavelengths as short as ~0.4μm is probably due to the contribution of high energy photons penetrating the extremely thin (~400Å) window layer; the energy of these short-wavelength photons is ~3.1eV, larger than the energy of the direct bandgap (2.8eV) of the $p^+Ga_{0.2}Al_{0.8}As$ window layer.

Thus, according to the spectral response curve of Figure 68, the structure actually achieved in this sample was $p^+Ga_{0.2}Al_{0.8}As/nGaAs/n^+GaAs/p^+GaAs/nGe$, forming a double-heterojunction cell connected by a conducting tunnel junction. This encouraging – although unexpected – result prompted additional MBE structures in this materials system to be grown having the desired layer configuration.

Shortly before the end of Phase 1 a hybrid GaAs-Ge two-cell SMBSC was prepared by a combination of MO-CVD and MBE techniques. This structure involved the growth of a window-type GaAlAs/GaAs solar cell structure at 750°C on a connecting n^+-p^+ tunnel junction in GaAs which was deposited by MO-CVD at 630°C on the surface of a Ge solar cell structure previously prepared by MBE techniques. The In metal layer applied to the back surface of the Ge wafer for the purpose of mounting the substrate with good contact in the MBE system (a standard procedure with substrates in that apparatus) had become alloyed into the Ge to an appreciable depth, and some difficulty was encountered in removing the In-containing layer completely prior to inserting it into the MO-CVD reactor.

Although the removal was eventually effected, the front surface of the Ge cell structure was slightly damaged, and this adversely influenced the growth of the five MO-CVD layers of the tunnel junction and the GaAs window cell. However, the large-area structure was completed (the Ge wafer was ~1-1/2 in. in diameter) with an 800Å $Ga_{0.1}Al_{0.9}As$ p-type window layer on a 1.4μm p-type GaAs:Zn layer on a 4.6μm n-type GaAs:Se base region; the conducting tunnel junction consisted of n^+GaAs:Se/p^+GaAs:Zn, with each layer ~0.3μm thick. Processing of this stacked cell was not completed by the end of Phase 1, however.

Additional SMBSC structures involving GaAs and Ge solar cells prepared by various combinations of MO-CVD and MBE techniques are expected to be fabricated and evaluated in Phase 2, commencing immediately at the start of the program. This combination of cells is of interest not only as a two-cell tandem assembly but also as the two lower-bandgap cells in a three-cell SMBSC consisting of GaAlAs, GaAs, and Ge cells in series (see Task 4 discussion).

2.3 GaAs-InGaAs SMBSC TECHNOLOGY DEVELOPMENT

This task was to involve the LPE growth of multiple-bandgap cell structures in the GaAlAs-GaAs system and the InP/InGaAs system to produce a two-cell SMBSC. Good overall efficiency was expected for this system, and it was anticipated that the series current-conduction problem at the interface between cells would be solvable by interface-defect tunneling. Most experimental cells were expected to be grown on GaAs substrates rather than on prohibitively expensive InP substrates, although some structures were to be prepared on InP substrates early in the program for making various critical comparisons.

As a first step in this task the LPE growth of p^+InP layers on n^+GaAs single-crystal substrates was to be undertaken. Growth conditions required for control of the InP surface morphology on such substrates were to be determined. Properties of the interfaces were to be investigated as functions of various growth parameters (temperature, doping concentrations, cooling rates) and of the growth sequence. The current conduction mechanism, expected to be dominated by interface-defect tunneling in this materials system, was to be investigated so that the layer growth conditions required for low-resistance ohmic conduction could be established.

When that was successfully achieved the growth of LPE layers of p- and n-type InGaAs on the p^+InP layers was to be undertaken. The photovoltaic properties of the InGaAs junction would then be determined, and deposition parameters would then be adjusted to optimize the photovoltaic performance for use in the two-cell (GaAs and InGaAs) system.

Next, growth of p- and n-type InGaAs LPE layers on p^+InP single-crystal substrates was to be investigated, and the photovoltaic properties of optimized InGaAs junction structures grown on such substrates compared with the photovoltaic properties of the devices grown on the p^+InP/n^+GaAs composites described above. This would indicate if further optimization of the InGaAs cells grown on the composites was required for use in the SMBSC assembly.

After satisfactory development of the LPE InGaAs cell structure on the p^+InP/n^+GaAs substrate, the complete two-cell assembly was to be fabricated by growing the GaAlAs/GaAs heteroface cell structure by LPE on the second (back) side of the same n^+GaAs single-crystal substrate. The photovoltaic properties of the two-cell stack would then be measured and evaluated, and any required modifications in fabrication procedure for the individual component cells would be developed. Finally, the overall growth and fabrication procedure was to be carefully assessed, and any indicated changes to optimize the photovoltaic performance of the complete assembly were to be developed and incorporated.

This task was also expected to involve the evaluation of various contact materials and configurations as required, as the work progressed.

2.3.1 InP and InGaAs Layers Grown by LPE

LPE growth experiments with heavily doped p^+InP layers were begun in the first month of the program, using n^+GaAs single-crystal substrates. However, the surface morphology of the initial InP films on GaAs was unsatisfactory. The effects of changes in growth temperature, degree of super-cooling of the melt, and cooling rate after growth were investigated in an attempt to improve the quality of the InP surfaces.

Preliminary LPE growth experiments were also begun at about the same time (in a separate apparatus) on the InGaAsP materials systems. Although this quaternary was intended for eventual use as the *1.0 eV cell material* for the LPE three-cell SMBSC (Task 5), exploratory experiments with growth of the small-bandgap (~0.7eV) ternary InGaAs were undertaken first.

Single-crystal substrates of p^+InP of two different orientations were also used for the experimental growth of n^+InP layers, as a preliminary step to growing $n^+InGaAs$ followed by $p^+InGaAs$ layers. These experiments were limited at the time to an evaluation of the effects of crystallographic orientation of the substrate upon the surface morphology of the InP films. Once a preferred orientation for the single-crystal InP substrate was identified – presumably one of the three orientations (100), (111A), (111B) – additional substrate wafers were to be prepared and some three-layer experimental structures grown.

The composition of InGaAs selected for use as the 0.7eV cell material was that which is lattice-matched to InP and has the approximate composition $In_{0.52}Ga_{0.48}As$. The use of an InP window for the small-bandgap cell should not cause serious absorption loss of usable solar radiation transmitted by the top cell (GaAs), since the bandgap energy of InP is only slightly smaller than that of GaAs. If the window material used for the small-bandgap cell has a significantly smaller bandgap energy than that of GaAs then appreciable absorption losses would result, so the choice of the window material (and thus the material on which to grow the small-bandgap cell structure) is quite restricted. Examination of appropriate bandgap-vs-lattice constant diagrams for various compositions of materials indicated that possible window materials include InGaP ($E_g \geq 1.4eV$), InGaAsP ($E_g > 1.4eV$), AlInAs, and GaAlInAs, in addition to InP itself.

The InP LPE growth experiments on GaAs continued with both In and Sn used as the solvent. Both the growth temperature and the cooling rate were varied, with the super-cooling of the melt maintained at 5 deg C. The results showed that InP layers with rather rough surfaces could be grown on (100)-oriented GaAs substrates using a Sn solution. The In solution, however, attacked the GaAs substrate severely, and melt was always left on the substrate at the conclusion of the growth experiment as a result of the rough growth surface.

Growth experiments were then begun with both In and Sn solutions and (111B)-oriented GaAs substrates, since it had been recently reported that acceptable LPE growth of InP on this GaAs plane can be achieved, and good quality epitaxial growth of InP was obtained on this plane previously by MO-CVD at Rockwell ERC. The substrates were "cooled" during the deposition process to maintain their temperatures below the normal temperature induced by the process. This procedure appeared to offer some promise. It was shown that LPE growth at 800°C resulted in much less In inclusion at the InP-GaAs growth interface than was obtained at 600°C, but the grown layer had a smoother surface for the 600°C growth than for 800°C growth. Subsequent experiments showed that the growth temperature was very critical for growth from In solution, with the optimum temperature appearing to be about 520°C, with departures from this by as little as 30 deg C (above or below) causing severe problems with melt wipe-off.

Several InGaAs p-n junction structures were also grown by LPE on (111B)-oriented single-crystal n^+InP substrates. The grown layers were generally smooth but exhibited small pits in areas away from the crystallographically on-orientation plateaus. The density of these pits was rather low, however, so it was believed that the photoresponse of the junction devices might not be seriously affected.

Several of the InGaAs p-n junction structures prepared in these experiments were evaluated by preparing small-area (~0.025 cm^2) mesa devices. Contact to the p-type InGaAs layer was made by vacuum-deposited Ag-Zn pads, and the n^+InP substrate was contacted by means of vacuum-deposited Au-Ge on Pt. The Ag-Zn contact on the p layer did not result in low contact resistance, however, and it further exhibited a tendency to ball-up and not wet the InGaAs layer surface during the post-deposition heating cycle.

Figure 69 shows the measured relative spectral response for one of these devices when the monochromatic light was incident on the InP substrate side. An absolute quantum efficiency of ~20 percent was measured with a 1.06μm laser and a calibrated reference diode. This low value indicates that the minority-carrier diffusion length in the grown InGaAs layer was probably quite low. The typical layer thickness for these growths was also on the low side (< 2μm), resulting in fast drop-off of the photoresponse at the long-wavelength end. Also, since Zn was used as the acceptor impurity in these structures, Zn contamination of the n-type melt was probably taking place, and some Zn diffusion out of the p-type layer probably also occurred during cooling after the growth process was complete, giving rise to the question of whether the deposited n-type InGaAs layer actually survived the complete growth process or not.

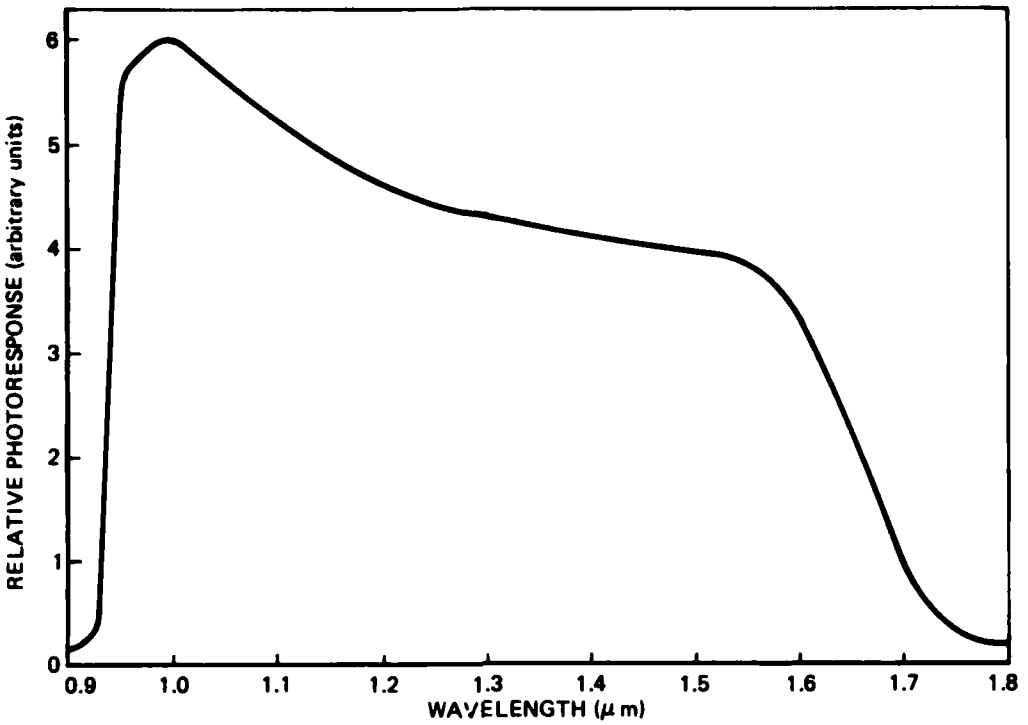


Figure 69. Spectral Photoresponse of LPE InGaAs p-n Junction Cell with Illumination Incident through InP Substrate

The dark I-V characteristics of these devices showed high values for n (close to 3), indicating that the current transport was not the ideal type (injection over the p-n junction barrier). Although the temperature dependence of the I-V characteristics was not measured, it was expected that current transport in these devices was of the defect-assisted tunneling type that has been observed in many heterojunction device structures; that is, it appeared that a heterojunction between InP and InGaAs had resulted, rather than a simple p-n junction in InGaAs.

Figure 70 shows the measured dark and illuminated I-V characteristics of one of the mesa devices as measured using a curve tracer and a microscope lamp for illumination. The open-circuit voltage of >0.3V and short-circuit current of ~2mA are close to the expected values; however, the poor fill-factor was due to the excess forward current caused by the defect-assisted tunneling mentioned above.

To correct this situation new structures were grown with the goal of obtaining thicker InGaAs layers adjoining the substrates. One such experiment produced an n-type layer 1.5μm thick and a p-type layer 1.9μm thick. However, preliminary measurement of the photovoltaic properties indicated very weak photoresponse, for reasons not known. The possibility that poor ohmic contacts were involved and thus rendered the photovoltaic response measurements invalid led to the fabrication of complete devices with proper contacts for further evaluation. These also exhibited unsatisfactory photovoltaic properties, however.

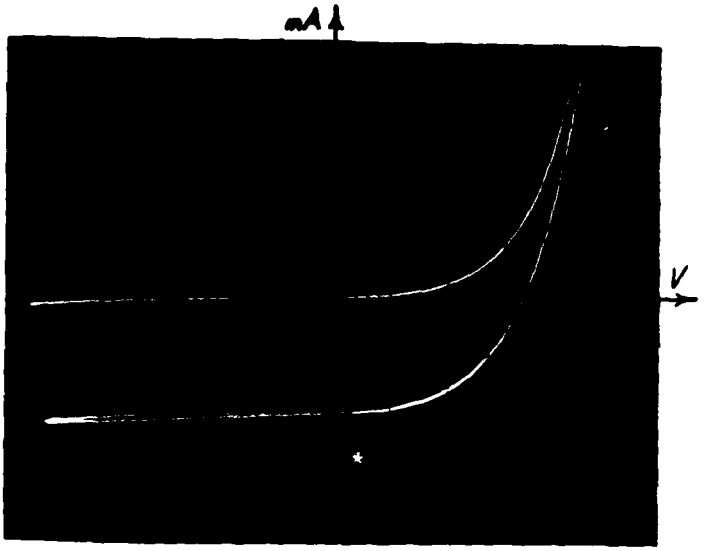


Figure 70. Dark and Illuminated I-V Characteristics of InGaAs p-n Junction Measured with Microscope Lamp Illumination ($V_{oc} > 0.3V$, $I_{sc} \approx 2mA$)

In an attempt to circumvent some of the LPE growth problems encountered in this materials system, experiments were planned in which InP n-type layers that had been previously grown on single-crystal GaAs substrates by the MO-CVD process would be used as growth surfaces for the LPE growth of InGaAs. Samples in which the MO-CVD InP layers were 2-6 μm thick were obtained, to attempt to reduce the effects of InP decomposition and avoid complete dissolution of the n-type layer during the initial etch-back stage in the LPE growth process. Subsequently, a special group of InP layers was prepared by the MO-CVD process with thicknesses ranging from 7.5 to 10 μm, to further alleviate this problem.

First, however, in preparation for LPE growth experiments with these substrates, several InP deposition experiments were done with bulk InP substrates at very low temperatures – below 500°C – using In solutions. These preliminary runs were considered necessary to minimize the possibility of losing the first group of relatively thin MO-CVD InP layers during the etch-back step. Unfortunately, good quality InP growth was not achieved in these experiments with bulk substrates.

Since early in the program, a number of experiments had been carried out with the LPE growth of InP on GaAs substrates. The experiments had involved growth from both In and Sn solutions, growth on (100) and (111) A and B surfaces, growth temperatures from 600 to 800°C, and the use of large vertical temperature gradients across the liquid-solid interface to minimize etch-back and enhance growth in a

nonequilibrium situation. While some of the InP layers appeared adequate for subsequent InGaAs epitaxial growth, examination of the structures under an infrared transmission microscope revealed large numbers of In inclusions completely opaque to near-IR radiation. Thus, while such InP layers might prove to be an adequate substrate for subsequent InGaAs growth, the interface problem would prevent their use in a stacked multiple-bandgap solar cell configuration. That is the situation that directed attention to the growth of InGaAs on InP and on a GaAs substrate which previously had an MO-CVD InP layer grown over its surface.

Since most of the initially available MO-CVD InP layers were relatively thin ($\leq 5\mu m$) it was necessary to grow at very low temperatures to avoid InP decomposition prior to epitaxial growth. Growth of InP at 450°C proved very difficult because of the low P solubility in In at that temperature. However, InGaAs growth at that low temperature was expected to be easier because of the higher As solubility in InP.

LPE growth of an $In_{0.47}Ga_{0.53}As$ layer was undertaken on one of the thicker InP/GaAs composite samples previously prepared by MO-CVD. The undoped n-type InP layer had been deposited at ~725°C on a (111B)-oriented GaAs substrate, with a resulting InP thickness of ~7.5μm. The resulting InGaAs layer grown by LPE was found to be spotty and discontinuous, with very poor melt wipeoff. This result was believed to be due simply to the extreme caution that was exercised to prevent excessive meltback of the CVD InP layer and the possible consequent melt attack of the underlaying GaAs substrate. The absence of meltback apparently permitted retention of oxides and other impurities at the growth interface, thus interfering with the epitaxial growth process.

The next experiments were done with bulk crystal InP substrates rather than the CVD layers until the LPE growth parameters were more satisfactorily defined. Successful growth of an InGaAs layer by LPE was achieved with (111B)-oriented p^+InP single-crystal substrates that were lapped to an acceptable thickness and then polished prior to the deposition experiments.

Growth was accomplished by contacting the substrate to the melt at a temperature ~0.5 deg C above the measured saturation temperature. This procedure provided 0.5-1.0μm of substrate etch-batch and appeared to be a crucial factor in obtaining successful growth in this materials system. The grown layer was not intentionally doped, but subsequent electrical characterization indicated the layer to be n type. Growth was initiated at about 629°C and proceeded with a cooling rate of ~1 deg C per min. Under those conditions the average growth rate for the InGaAs was slightly above 1μm/deg C. The actual composition of the layer was not determined, but the general quality of the growth suggested there was close lattice match between the layer and the InP, implying a composition very close to $In_{0.47}Ga_{0.53}As$. The bandgap for such a composition would be 0.7eV – nearly identical to that of GaSb.

Although the InGaAs layer appeared mirror-like to the unaided eye, at high magnifications numerous lens-shaped surface features were visible. It was speculated that these may have resulted from the cooling rate being too rapid. Similar but more pronounced surface features have been reported by Sankaran et al (Ref 10)

and were attributed to local Ga concentration gradients and fluctuations at the growing interface caused by the large Ga distribution coefficient ($K_{Ga} \approx 6.12$) in this type of melt.

It was expected that a p-n junction had been formed in the grown n-type *InGaAs* layer due to the known rapid out-diffusion of Zn from the p^+InP substrate. One of the structures was processed into individual mesa-type solar cells (0.025 cm x 0.025 cm) for photovoltaic evaluation. The substrate was thinned to about 4 mils by a combination of lapping and etching to reduce the free-carrier absorption losses of photons entering the cell structure from the InP side prior to their reaching the p-n junction region in the InGaAs.

A full-coverage Au-Ge contact layer ~2000Å thick was applied to the n-type surface of the InGaAs layer and sintered at 450°C in H_2 for 1 min. Because of the problem that sometimes occurs in contacting p^+InP, several small pieces were taken from the as-grown composite structure for use in contact optimization experiments. With a pattern of 10-mil diameter dots used as a test grid it was found that satisfactory ohmic behavior was provided by contacts of Au(500Å)/Zn(500Å)/Au(1500Å) vacuum-deposited sequentially on the InP followed by sintering at 450°C in H_2 for 1 min. After preparation of the contacts by these techniques on the main part of the composite wafer it was then cleaved into individual 0.025 cm x 0.025 cm solar cells for testing.

These devices consistently exhibited short-circuit current densities of ~16mA/cm^2 and *open-circuit voltages of* < 0.1V under AM1 illumination (simulated). The very low V_{oc} values were believed to be caused by large dark saturation current densities and poor (i.e., high) diode factors. This view was supported by the strong observed sensitivity of V_{oc} to the incident light intensity. Using a focused microscope lamp as light source and varying the intensity of illumination on the cell it was possible to obtain data showing the variation of V_{oc} with J_{sc} over a reasonable range. The relation

$$V_{oc} = n\frac{kT}{q}\ \ell n\left(\frac{J_{sc}}{J_o} + 1\right)$$

was then used to determine that n=1.9 and $J_o \approx 4.75 \times 10^{-3}$ A/cm^2 for these devices. These values can be compared with those obtained for GaSb cell structures (see next section), for which n=1.7 and $J_o \approx 4 \times 10^{-4}$ A/cm^2.

Representative dark and illuminated I-V curves obtained with one of these cells using the microscope lamp are shown in Figure 71. The strong dependence of V_{oc} on incident light intensity is evident in the figure. The cause of the large J_o observed in the InGaAs devices was not identified. Some indication was found that *the structure may have contained* a weak blocking diode in addition to the main active p-n junction. However, more work is needed to establish if such a second diode (if present) is caused by a valence-band energy spike at the InP-InGaAs interface – perhaps formed during the LPE growth process – or is simply the result of subsequent steps in the cell fabrication process (see below).

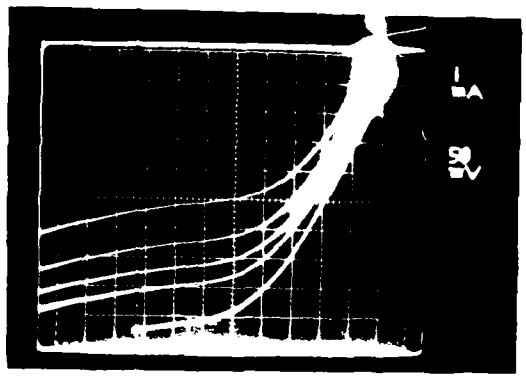


Figure 71. Dark and Illuminated (microscope lamp) I-V Curves Obtained for Different Intensities of Illumination for InP/InGaAs Solar Cell (0.025 cm x 0.025 cm) Obtained by LPE Growth of Undoped n-type InGaAs Layer on Single-crystal p^+InP Substrate Wafer (Illumination through thinned InP substrate)

Figure 72 shows a representative spectral response curve for this group of InP/InGaAs cells. Also shown in the figure for comparison is an equivalent photoresponse curve for a GaSb cell made earlier and described in the next section. The sharp cutoff in the response curve for the InGaAs cell at ~0.95μm is due to the 1.35eV bandgap of the InP window (the substrate, in this case). The long-wavelength cutoff at 1.65-1.70μm corresponds to a bandgap energy of ~0.75eV for the LPE-grown InGaAs layers – somewhat larger than the 0.7eV bandgap expected for the $In_{0.53}Ga_{0.47}As$ composition which is a lattice match for InP. The peak response observed at relatively short wavelength (~1.05 μm) for these cells tended to indicate that the cell may actually have consisted of a p-p^+ heterojunction at the interface of the p^+InP substrate and the LPE-grown layer of InGaAs, and a second junction – a shallow p-n junction – produced in the undoped but n-type InGaAs layer by the diffusion of Zn out of the InP substrate into the otherwise undoped layer as the LPE growth process proceeded. It was suspected that the apparent discrepancy in bandgap energy between the grown material and the lattice-matching composition may have been caused by incorporation of a small amount of P in the grown InGaAs as a result of the initial predeposition etch-back of the InP substrate.

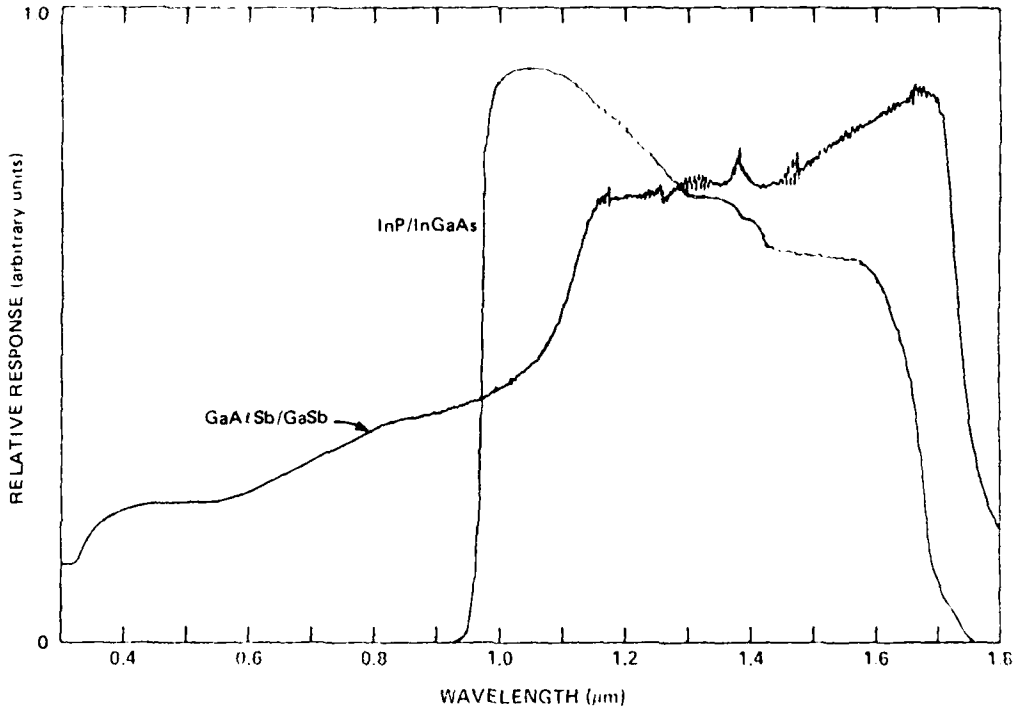


Figure 72. Relative Spectral Response Curve for InP/InGaAs Window-type Solar Cell Grown by LPE (InGaAs layer grown on InP substrate, with growth initiated at 629°C). Response Curve for GaAlSb/GaSb Cell Also Shown, for Comparison

Because of the decision to change the emphasis of the program late in Phase 1, no further work was done with this materials system beyond that described above. However, severe problems had emerged in the work with the InGaAs system before those activities were curtailed - including the difficulties in achieving InP layer growth on GaAs by LPE and the problems encountered in maintaining the InGaAs p-n junction at the desired location in multilayer structures because Zn was the only proven p-type dopant for this material and also diffuses rapidly in InGaAs. Consequently, an alternative materials system was sought, and the AlGaAsSb system was examined for this possibility. The efforts devoted to study of that system are summarized in the following section.

2.3.2 AlGaAsSb Materials System as Alternative for Low-bandgap Cell

This materials system covers the 0.7-1.6eV bandgap energy range and is a potential candidate for use in both low- and high-bandgap solar cells. Significant improvements had been realized in these materials at ERC Thousand Oaks in an avalanche photodiode application (Ref 11). These materials have the advantage that Ge and Sn are both p-type dopants with small diffusion coefficients in the quaternary alloys.

On the basis of this experience a preliminary examination of GaSb as a low-bandgap solar cell alternative was made. The structure used was AlGaAsSb(p)/GaSb(p)/GaSb(n), and the Al concentration in the window layer was 0.30, corresponding to a bandgap energy of 1.1eV. The GaSb(p) layers had hole concentrations of $p \approx 10^{17}$ cm^{-3} (undoped), with the substrate concentration $n=4\times10^{17}$ cm^{-3}.

Solar cells with grid contacts were fabricated on 0.025 cm^2 mesas. Figure 73 shows cell characteristics with and without an AlGaAsSb window layer. The windowed cell showed lower series resistance and higher short-circuit current density than the bare cell due to reduced surface recombination velocity and lower effective sheet resistance achieved with the AlGaAsSb window layer. The series resistance was still too high for good cell performance, however. The cause may have been either excessive contact resistance or high sheet resistance.

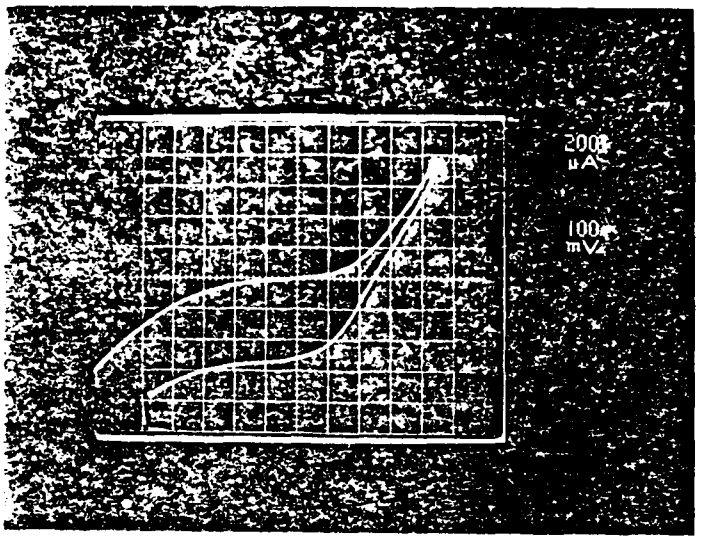
The measured V_{OC}, J_{SC}, FF, and η values for the first cell under AM1 solar simulator illumination were 0.25V, 20.8 mA/cm^2, 0.37, and 1.9 percent, respectively. The cell thus exhibited quite good J_{SC} and V_{OC}, and improvements in fill factor could lead to a usable 0.7eV cell. This was an encouraging first attempt, justifying further investigation of this materials system.

Figure 74 shows the spectral response curve for the window-type cell of Figure 73a, showing cut-off wavelengths at 1.1μm and 1.7μm, corresponding to the bandgaps of the AlGaAsSb window layer and the GaSb layers, respectively. The reduced response in the short-wavelength region suggests that the p-GaSb layer was too thick (the thickness was measured to be ~10μm).

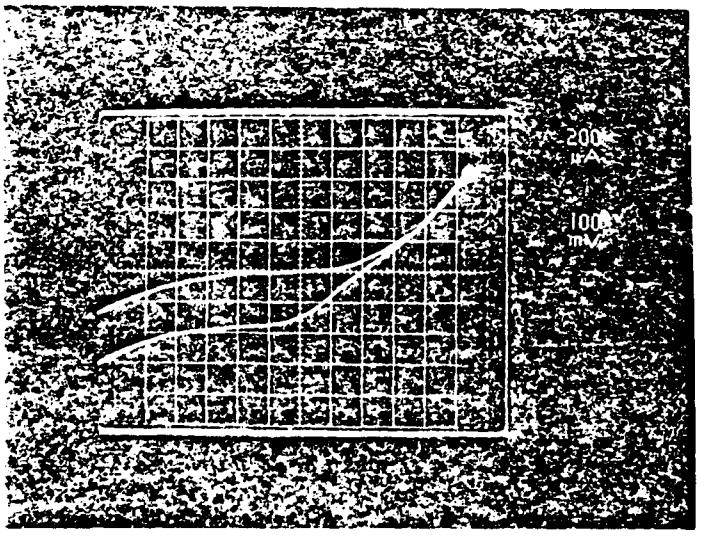
Attempts were made to reduce the p-layer thickness in the GaSb cell and to improve the cell contacts to achieve lower series resistance in the experimental cells.

Reduction in the p-layer thickness was achieved by using shorter layer growth times coupled with minor Al additions to the GaSb which reduced the layer growth rate and resulted in a composition of approximately $Ga_{0.9}Al_{0.1}Sb$. The resulting p-layer thicknesses were in the range 2-3μm for the alloy, in contrast to the 10μm thickness obtained in the first GaSb layers described above. Typical LPE growth times and temperatures were 1 min at 520°C for the p-type $Ga_{0.9}Al_{0.1}Sb$ layers and 2 min at 520°C for the p-type GaSb grown first.

Table 6 summarizes the pertinent material parameters for three of the structures with thin p layers and two of the previous structures with thicker p layers. Also included in the table are the properties of typical individual mesa-type solar cells (0.025 cm^2 area) fabricated in each of the composite structures listed. The best of the cells is seen to be the last one listed in the table; it exhibited a short-circuit current density J_{SC}=28.8 mA/cm^2, open-circuit voltage V_{OC}=240mV, fill factor of 0.51, and conversion efficiency of 3.5 percent for simulated AM1 illumination of 1 sun intensity and with no AR coating applied. Such values are in the range expected for devices which respond only to the portion of the solar spectrum between 0.85 and 1.1eV. The prospects thus seemed relatively good for ultimately producing an optimized small-bandgap (0.7eV) cell with a 1.45eV window layer for use in conjunction with the GaAlAs/GaAs cell in a two-cell SMBSC.



(a)



(b)

Figure 73. Dark and Illuminated (AM1 simulator) I-V Characteristics of pGaSb/nGaSb Solar Cell (area 0.025 cm^2) a) with AlGaAsSb Window Layer and b) without Window Layer

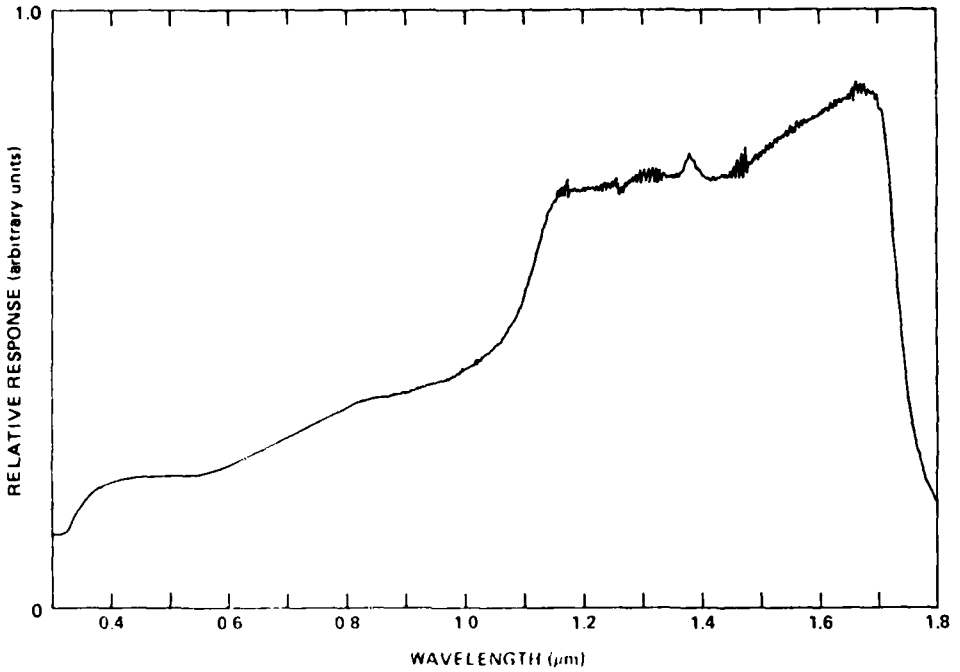


Figure 74. Spectral Response of pAlGaAsSb/pGaSb/nGaSb Window-type Solar Cell of Figure 73a.

Figure 75 shows the dark and illuminated I-V characteristics for the three individual cells having thin p-layers. It is evident from these curves that there were both junction leakage and series resistance problems in varying degrees in these cells.

Dark log I-V data were also obtained for these cells, and the diode factors and dark saturation-current values derived from those measurements were found to be typically n=1.7 and J_o 10^{-4} A/cm^2, respectively. Calculation of expected V_{OC} values using these measured parameters and measured values of J_{SC} indicated good agreement with the previously measured V_{OC} data. The values obtained suggested somewhat better junction quality was realized in these LPE-grown diodes than in diodes reported earlier by Sukegawa et al (Ref 12), for which n=1.87 and $J_o=3\times10^{-4}$A/cm^2 at voltages less than 0.18V, and n=2 and $J_o=1.5\times10^{-3}$A/cm^2 at voltages greater than 0.18V were obtained.

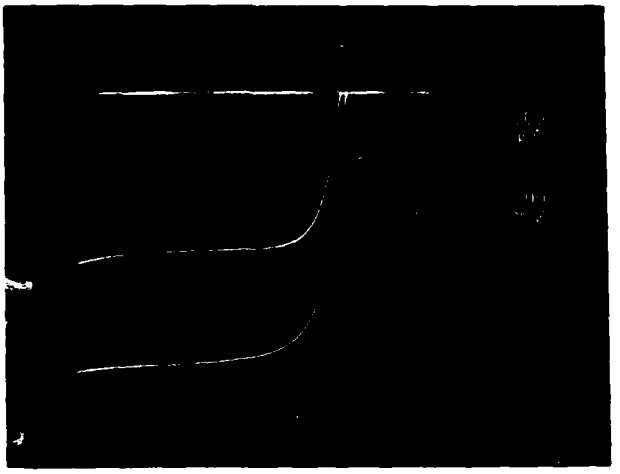
The need for low contact resistance prompted an examination of various contacting materials for both p-type and n-type GaSb. The results of this brief experimental study are summarized in Table 7. As can be seen from the data, pure Au produced the lowest contact resistance for both conductivity types. It is interesting that solar cell No. 119 M-6 #1 (see Table 6), which had Au contacts to both regions of the cell, had the poorest V_{OC} of any of the devices listed. This suggested there may have been a low shunt resistance associated with this type of contact.

Table 6. Material, Fabrication, and Typical Individual Cell Photovoltaic Performance Parameters for Window-type Solar Cell Structures Grown by LPE on n-type GaSb Single-crystal Substrates*

Approx. p-layer Thickness (μm)	p-layer Composition	p-layer Doping (cm-3)	p-layer Growth Time (min)	p-layer Growth Temp. (^{o}C)	p-layer Contact Material	n-layer Contact Material	Typical Individual Cell† PV Response**				
							Cell No.	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF	η (%)
10	GaSb (no window)	$1x10^{17}$	2	520	Au-Ge,Pt,Au	Ag-Mn,Pt,Au	116	200	12.0	0.29	0.7
10	GaSb (with window)	$1x10^{17}$	2	520	Au-Ge,Pt,Au	Ag-Mn,Pt,Au	115	250	20.8	0.37	1.9
3	$Ga_{0.9}Al_{0.1}Sb$	$3.7x10^{17}$	1	520	Au	Au	119 M-6 #1	160	13.6	0.37	0.8
2	$Ga_{0.9}Al_{0.1}Sb$	$8x10^{16}$	1	520	Au-Ge,Pt,Au	Au	118 M-5 #4	200	22	0.52	2.3
2	$Ga_{0.9}Al_{0.1}Sb$	$8x10^{16}$	1	520	Au-Ge,Pt,Au	Ag-Mn,Pt,Au	118-1 M-4 #2	240	28.8	0.51	3.5

*Cell configuration: $p^{+}Ga_{0.7}Al_{0.3}AsSb/pGa_xAl_{1-x}Sb/nGaSb$ (substrate).
†Cell area 0.025 cm^2 (mesa).
**Simulated AM1 illumination, no concentration.

(a) (b)



(c)

Figure 75. Dark and Illuminated (AM1 simulator) I-V Characteristics of LPE-grown $p^{+}GaA\ell AsSb/pGaA\ell Sb/nGaSb$ Window-type Solar Cells (Table 6). a) No. 119 M-6 #1; b) No. 118 M-5 #4; c) No. 118-1 M-4 #2 (All cell areas 0.025 cm^2)

Table 7. Summary of Materials and Fabrication Parameters Used in Investigation of Various Ohmic Contacts to p-type and n-type GaSb

	n-type GaSb			p-type GaSb				
Materials	Au-Ge	Pt	Au	Sn	Au	Ag-Mn	Pt	Au	Au	
Thickness (Å)	2000	150	100	1500	3000	2000	150	1000	3000	
Sample Temp. during Contact Deposition* (°C)	RT**			RT**	200	RT**			200	
Contact Alloy Temp. (°C)	400			400	400	300			Not heat treated	300
Contact Alloy Time (min)	2			1	1	2			–	2
Contact Dot Area (cm^2)	$2x10^{-3}$			$5x10^{-4}$	$5x10^{-4}$	$1.45x10^{-3}$			$5x10^{-4}$	$5x10^{-4}$
Contact Specific Resistance (ohm-cm^2)	$5x10^{-3}$			$4.8x10^{-3}$	$4.4x10^{-4}$	$4.35x10^{-3}$			$1.8x10^{-3}$	$1.5x10^{-3}$

*Contact materials vacuum-deposited
**RT = room temperature

Additional attempts were made to grow window-type cell structures with higher Aℓ composition (~0.7) in the window layer, but a series of apparatus problems occurred that seriously delayed progress for a time. Those difficulties were resolved and additional GaAℓSb/GaSb cell structures were again successfully grown and processed into solar cells late in Phase 1, at about the time the shift in program emphasis was adopted.

As a result, no further work was done with this materials system in the Phase 1 program.

2.4 GaAℓAs - GaAs - GaAsSb SMBSC TECHNOLOGY DEVELOPMENT

This task was initially planned to involve growth of the three individual cell components by the MO-CVD process, with subsequent integration of the three into a single SMBSC assembly. It was anticipated that single-crystal GaAs would be used as the substrate for the composite structure and that each of the three cells would be grown with an appropriate window material. Because of the complexity of the three-cell SMBSC and the fact that little was known about 2.0eV GaAℓAs cells or 1.0eV GaAsSb cells, individual materials properties as well as the properties of each of the cell structures were to be extensively characterized as this task progressed.

The conduction properties of n^+-p^+ junctions prepared in GaAℓAs composite layer structures were to be studied for various MO-CVD growth conditions. Deposition parameters resulting in high interface doping concentrations and abrupt transitions in doping impurity were to be determined, so that the required low-resistance nonrectifying junctions could be achieved in GaAℓAs.

Single-crystal n^+GaAs substrates were then to be used for the MO-CVD growth of GaAℓAs layers successively doped n and p type to produce a 2.0eV p-n junction solar cell in the alloy. This was expected to require considerable experimentation with both layers; although the GaAℓAs alloy system was already extensively developed by both MO-CVD and LPE and has an available lattice-matched window, the 2.0eV composition is close to the direct-indirect gap crossover composition and the minority carrier properties are not well known in this composition region. However, GaAℓAs can be grown with compositions throughout the entire range by MO-CVD, so the required layers were to be prepared and their pertinent materials properties--including minority carrier diffusion length and surface recombination characteristics--determined to assist in evaluation of this alloy system for the 2.0eV cell material. The characteristics of the p-n junction cells resulting from these investigations were also to be determined, to complete the evaluation.

Upon successful development of a satisfactory GaAℓAs 2.0eV cell, that structure was to be combined with the well-developed GaAℓAs/GaAs solar cell structure on a single n^+GaAs substrate, utilizing the nonrectifying n^+-p^+ tunneling junction in GaAℓAs mentioned above and planned for development earlier in the program. The MO-CVD growth sequence was expected to involve first the deposition of the conventional GaAℓAs/GaAs cell (with a p^+ upper layer) on the n^+GaAs substrate,

followed next by deposition of the n^+/p^+ connecting junction, and then by deposition of the 2.0eV p/n GaAlAs cell. Deposition parameters were to be optimized to achieve the best photovoltaic performance for this two-cell SMBSC assembly, which would then be used in the complete three-cell structure to fabricated later.

The 1.0eV cell material originally planned for development for use in this three-cell SMBSC was the GaAsSb alloy system, already discussed in Section 2.3.2. GaAs single-crystal substrates were to be used for growth of p- and n-type GaAsSb layers by the MO-CVD technique. The required 1.0eV bandgap corresponds to the composition of $GaAs_xSb_{1-x}$ for which $x \approx 0.5$, with a lattice constant of about 5.82Å. Although this alloy composition had not been grown by MO-CVD, little difficulty was anticipated in achieving such material. When satisfactorily doped layers of both types were obtained the two were to be combined to produce p-n junction cells of the desired bandgap and the deposition parameters adjusted to provide satisfactory photovoltaic performance. Lattice-matched GaAlAsSb window layers would then be prepared (also by MO-CVD) for this 1.0eV cell structure and the overall photovoltaic properties determined.

It was anticipated that once the MO-CVD GaAsSb 1.0eV cell was satisfactorily developed it would then be possible to combine all of the structures into a single three-cell SMBSC. To accomplish this the 1.0eV cell would be grown by MO-CVD on the second (back) side of the n^+GaAs substrate that was also used for the growth of the two-cell (GaAlAs and GaAs) SMBSC configuration on its front surface. Attention was to be given to achieving the required nonrectifying conducting interface between the n^+GaAs substrate and the heavily doped p^+GaAlAsSb window layer of the 1.0eV cell. The deposition sequence, layer thicknesses, specific layer compositions and doping concentrations, MO-CVD growth parameters used in preparing the three-cell composite, and matarials and processes used for producing low-resistance ohmic contacts were then to be examined, and the overall fabrication process modified as needed to produce the desired photovoltaic performance in completed three-cell SMBSC structures. (Some of these areas were investigated as part of the LPE work done with this materials system in Task 3, described in Section 2.3.2.)

Partly because the properties of 2.0eV GaAlAs and 1.0eV GaAsSb were not well known at that time and partly because InGaP and InGaAsP had both been grown as thin films and fulfill the bandgap requirements for the 2.0eV and 1.0eV cell materials, respectively, these two materials prepared by MO-CVD were considered alternates for possible use in the three-cell SMBSC assembly. Such parallel studies, if undertaken, would occur at a much lower level of effort than the primary activity. Solar cell junction structures of each material would be grown on single-crystal GaAs substrates by MO-CVD techniques, and the measured photovoltaic properties of such devices would be compared with those of the GaAlAs and the GaAsSb cells. If continuing serious difficulties were encountered in achieving the required performance for the GaAlAs cell and/or the GaAsSb cell then either or both of the In system materials would be further developed as substitutes.

This initial overall plan for this task was modified late in the Phase 1 program, when the change in program emphasis was adopted. For the balance of Phase 1 the work of the task was restricted to the GaAlAs-GaAs two cell SMBSC configuration and to the possibility of a GaAlAs-GaAs-Ge three-cell SMBSC assembly.

The activities of this task in the Phase 1 program are summarized in the following sections.

2.4.1 GaAlAs Solar Cells

Growth of the 2.0eV GaAlAs cells needed for the three-cell SMBSC to be developed using MO-CVD techniques required accurate calibration and control of the composition of the GaAlAs layers. Installation of a new source tank of trimethylgallium (TMG) on the reactor system used initially for this work made it necessary for several deposition experiments devoted to checking both the background impurity level in pure GaAs films grown with the new source and the dependence of the alloy composition (i.e., the value of x in $Ga_{1-x}Al_xAs$) upon the relative flow rates of the TMG and trimethylaluminum (TMAl) reactants.

Alloy films with $0.12 \lesssim x \lesssim 0.80$ were grown and characterized for composition by x-ray double-crystal diffractometer measurements and – for those films with composition in the direct-bandgap region – by room-temperature photoluminescence measurements of the energy gap. The results of the two measurements were found to correlate very well and the compositions thus determined indicated that the calibration of reactant concentration (i.e., flow rate) versus expected layer composition was quite accurate for this alloy system.

A malfunction of the MO-CVD epitaxial reactor used for growth of GaAs and GaAlAs structures occurred early in the program. The mass flow controller that controlled the TMAl flow rate into the deposition chamber began functioning incorrectly and so was replaced; several performance checkout runs were made to reestablish the parameters required for obtaining the appropriate alloy composition.

Additional $Ga_{1-x}Al_xAs$ p-n junction structures were then grown, primarily with $x = 0.37$ and at ~750°C. These were found to exhibit good I-V characteristics. Figure 76 shows the dark and illuminated (microscope lamp) I-V curves for a mesa diode (50 mil x 50 mil) fabricated in a junction structure in $Ga_{0.63}Al_{0.37}As$. The relatively small photoresponse shown is due in large part to the fact that the device did not have a window layer of $Ga_{1-x}Al_xAs$ (with $x \geq 0.8$) to reduce the effects of the high surface recombination velocity. However, the diode I-V curve shape is quite good.

Subsequently, along with the preparation of experimental tunneling junction structures in $Ga_{1-x}Al_xAs$ at lower deposition temperatures (see Section 2.4.2), p-n junction devices were also grown in $Ga_{1-x}Al_xAs$ at ~700°C rather than at ~750°C. These structures involved p-type and n-type $Ga_{0.6}Al_{0.4}As$ ($E_g = 1.92eV$) grown by MO-CVD on GaAs:Si substrates. A thin p+ GaAs:Zn cap layer was grown on top of the GaAlAs p-n junction structure to permit good ohmic contact to be made. The wafers were processed into 50 mil x 50 mil mesa diodes with 25 mil x 25 mil contact pads, and the I-V curves were examined with the curve tracer and mechanical probe contact. Good I-V characteristics were obtained, as indicated by the representative curve shown in Figure 77.

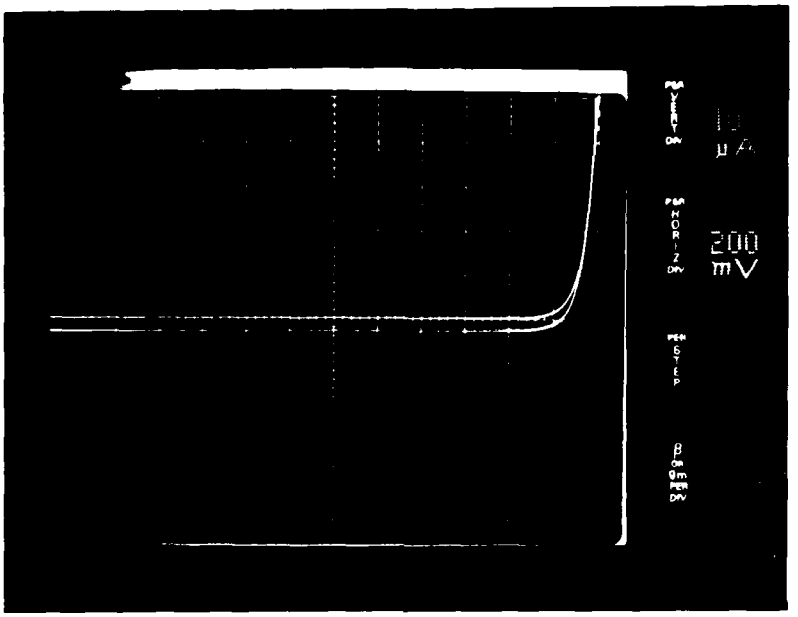


Figure 76. Dark and Illuminated (microscope lamp source) I-V Characteristics of 50 mil x 50 mil Mesa Diode Fabricated in $Ga_{0.63}Al_{0.37}As$ p-n Junction Structure Grown by MO-CVD on (100)GaAs Substrate (No window layer on this device)

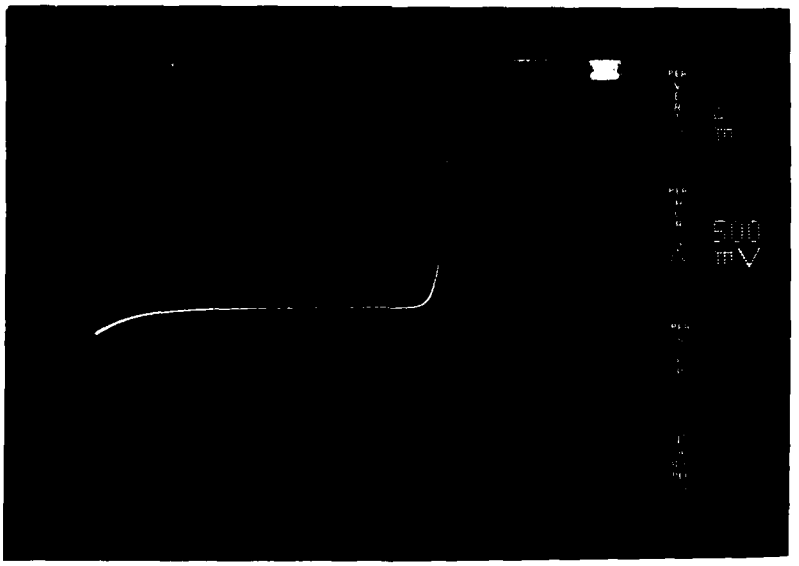


Figure 77. I-V Characteristic of p-n Junction Mesa Diode in $Ga_{0.6}Al_{0.4}As$ Structure Grown by MO-CVD on GaAs:Si Substrate (mesa 50 mil x 50 mil)

The first GaAlAs window-type solar cell structure was prepared by MO-CVD at about the same time. This structure involved a $Ga_{0.6}Al_{0.4}As$ p-n junction with a p-type $Ga_{0.2}Al_{0.8}As$ window layer and a thin p+GaAs cap layer for contact, all grown on a GaAs:Te substrate at 700°C. Individual 0.5cm x 0.5cm cells were processed on this wafer and characterized with microscope lamp illumination. The GaAs cap layer was then removed (except under the contact pattern) by etching in H_2O_2 (30 percent) - NH_4OH(pH 7.0) solution and the cells were again characterized.

As expected, the short-circuit current densities were observed to increase after removal of the cap layers, although the magnitude of the J_{sc} values remained relatively small. A typical set of dark and illuminated I-V curves for one of these individual 0.5cm x 0.5cm cells after removal of the cap layer is shown in Figure 78. The observed behavior was consistent with the discussion of the expected properties of this type of cell in the original program proposal.

Additional window-type GaAlAs cell structures were grown during the eighth and ninth months of the Phase I program. Most of the cells involved a $Ga_{0.7}Al_{0.3}As$ p-n junction with a p-type $Ga_{0.2}Al_{0.8}As$ window layer, grown in sequence on a GaAs:Te substrate. No contacting GaAs cap layer was used on these structures. The configuration, with dimensions, is shown in Figure 79.

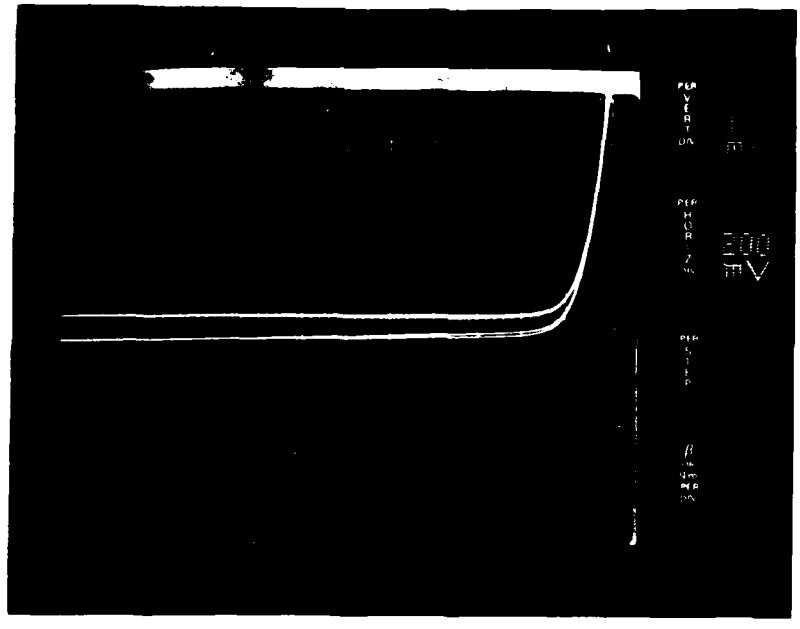


Figure 78. Dark and Illuminated (microscope lamp) I-V Curves for Thin-window Solar Cell (0.5cm x 0.5cm) in $Ga_{0.6}Al_{0.4}As$ Grown by MO-CVD at 700°C on GaAs:Te Substrate

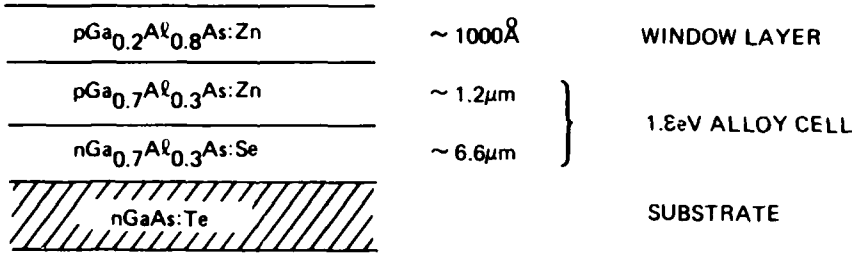


Figure 79. Configuration of $Ga_{0.7}A_{0.3}As$ Window-type Solar Cell Structure Grown by MO-CVD on GaAs Substrate

Cell structures in this configuration were grown at 700, 750, and 790°C. The wafers were processed in the usual way to make arrays of 0.5cm x 0.5cm individual cells; the cells were tested before sawing the wafers, using the microscope lamp illumination. It was found that the cell response improved generally with increasing deposition temperature. The maximum short-circuit currents observed for individual 0.5cm x 0.5cm cells under the "standard" microscope lamp illumination were ~200μA, ~500μA, and ~6mA for structures grown at 700, 750°, and 790°C, respectively.

Dark and illuminated I-V curves for one of the cells on a structure grown at ~790°C are shown in Figure 80. The V_{oc} for this cell is ~1.2eV, consistent with the ~1.8eV bandgap for this particular material. The photovoltaic properties of this cell are seen to be significantly better than those of the $Ga_{0.6}Al_{0.4}As$ cell grown at 700°C, as shown in Figure 78.

One of the later structures grown at ~750°C had an approximate alloy composition $Ga_{0.76}Al_{0.24}As$, and 0.5cm x 0.5cm cells processed in that sample exhibited V_{oc} values of ~1.2V and short-circuit currents $I_{sc} \approx 4.4$mA under microscope lamp illumination. Thus, cells with slightly lower Aℓ fraction showed somewhat improved performance relative to the $Ga_{0.7}Al_{0.3}As$ cells and much better properties than the $Ga_{0.6}Al_{0.4}As$ cells made previously.

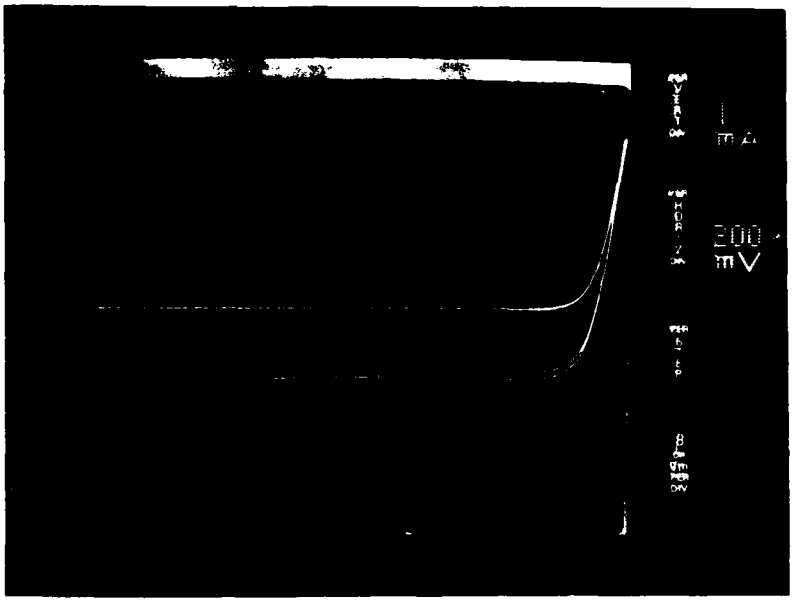


Figure 80. Dark and Illuminated (microscope lamp) I-V Curves for Window-type $Ga_{0.7}Al_{0.3}As$ p-n Junction Solar Cell (0.5cm x 0.5cm) Grown by MO-CVD at ~790°C on GaAs:Te Substrate

At about the same time that the above alloy cells were being made and tested, the first two-cell GaAlAs-GaAs SMBSC's were grown by the MO-CVD process (see Section 2.4.3) and characterized. The observed responses of those stacked assemblies indicated that the $Ga_{1-x}Al_xAs$ cells were probably limiting the overall response. Thus, improvement of the properties of the alloy cell became a primary activity of this task for the remainder of Phase I.

In the tenth month of the program another series of $Ga_{1-x}Al_xAs$ cell structures was grown, with $x \approx 0.30$ and a thin window layer of $Ga_{0.1}Al_{0.9}As$. These structures were deposited at 750°C, with the same layer thicknesses and doping concentrations as were used for the top cell of the GaAlAs-GaAs two-cell SMBSCs that were grown at about the same time. The wafers were processed exactly as conventional GaAlAs-GaAs heteroface solar cells; that is, the p contact was applied directly to the $Ga_{0.7}Al_{0.3}As$:Zn layer.

The I-V curves for a typical individual 0.5cm x 0.5cm cell on one of these wafers are shown in Figure 81. The value of the short-circuit current is seen to be only about 0.07 times that obtained for a typical conventional GaAs window cell under the same conditions of illumination with the microscope lamp (i.e., $I_{SC} \approx 10mA$). However, the illuminated I-V curve shown is similar to those obtained for other $Ga_{0.7}Al_{0.3}As$ cells grown earlier at the same deposition temperature.

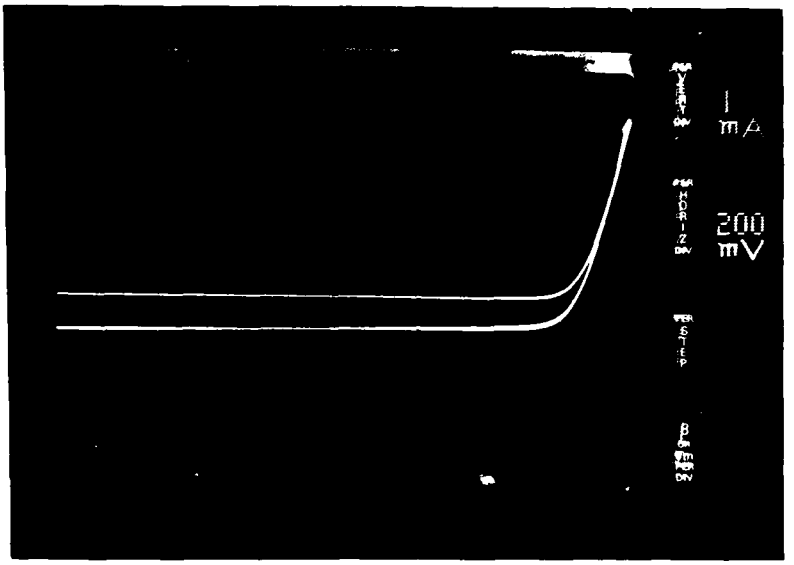


Figure 81. Dark and Illuminated (microscope lamp) I-V Curves for 0.5cm x 0.5cm Window-type $Ga_{0.7}Al_{0.3}As$ p-n Junction Solar Cell Grown by MO-CVD at 750°C on GaAs Substrate

Spectral response measurements were made on some of these alloy cells, and the results indicated a reduced short-wavelength response that was clearly a major factor in the low current density being obtained in the both the alloy cells and the two-cell GaAlAs-GaAs SMBSC's being made at the time. The spectral response measurements were made using a new probe-contact mounting fixture fabricated for use with the spectral response apparatus. The new fixture made it possible to obtain spectral response data for individual cells of an array of cells processed on a single substrate without separating the individual cells and mounting each on a separate header, as had been necessary previously.

Figure 82 shows spectral response data for two individual 0.5cm x 0.5cm alloy cells of composition $Ga_{0.7}Al_{0.3}As$ grown at 750°C on the same GaAs substrate. The high degree of coincidence of the point-by-point spectral response data for the two cells attests to the excellent uniformity of results obtained with the MO-CVD process over relatively large areas. The long-wavelength response cutoff corresponds to the expected bandgap of ~1.8eV for alloy of this composition.

However, the severely reduced high-energy response indicates that there was a serious problem with either carrier diffusion lengths or surface recombination effects in these cells, which had no window layer, a p layer 1.1μm thick,

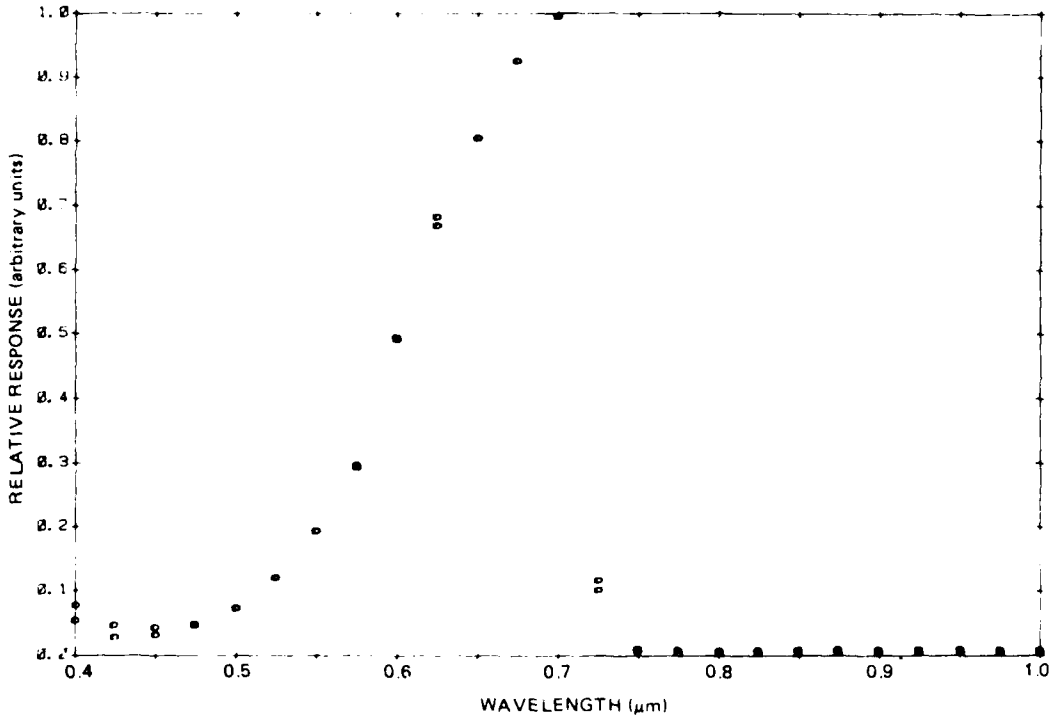


Figure 82. Spectral Response Data for Two 0.5cm x 0.5cm $Ga_{0.7}Al_{0.3}As$ Alloy Solar Cells Grown by MO-CVD at 750°C on Common GaAs:Si Substrate

and an n layer 3.0μm thick grown on a 0.4μm Se-doped buffer layer. In any case there was certain to be a major effect on the overall photocurrent realized from such a cell or from a two-cell SMBSC of which such a cell was a component.

One of the GaAlAs window-type cell structures that had been grown in the ninth month of the program, with the general configuration shown in Figure 79, was among the first cells characterized in detail in the new computerized solar cell measurements facility assembled at ERC Thousand Oaks during Phase 1 of this program. This particular sample consisted of an array of processed 0.5cm x 0.5cm individual cells grown on a large substrate wafer of 12-mil GaAs:Te. The sample had been left with Air Force APL personnel for examination at the time of a contract review in the twelfth month of the program and was subsequently returned to Rockwell for further use.

The structure involved a thin (~1000Å) window layer of p-type $Ga_{0.2}Al_{0.8}As$ on a $Ga_{0.76}Al_{0.24}As$ p/n junction cell grown on a 0.2μm n-type (Se-doped) GaAs buffer layer deposited on the substrate; there was no GaAs cap layer. The p-type active layer of the cell was ~0.6μm thick and the n-type region 2.4μm thick. All layers were deposited at ~750°C.

Dark and illuminated (microscope lamp) I-V curves for one of the individual cells on this sample, measured soon after it was first fabricated, are shown in Figure 83. The V_{OC} value for this illumination is 1.04V and the I_{SC} value 4.5mA (J_{SC} = 18mA cm^{-2}).

The photovoltaic properties of another cell on this same sample were examined by APL personnel using the APL AM0 simulator, prior to the sample subsequently being returned to Rockwell. Those preliminary measurements indicated an I_{SC} value of 2.1mA (J_{SC} = 8.1mA cm^{-2}) for AM0 illumination.

The measurements later made on one of the cells on this same sample, using the automated equipment at Thousand Oaks, produced the illuminated I-V characteristic shown in Figure 84 (for AM0 illumination). The principal parameters are V_{OC} = 0.96V, J_{SC} = 12.0mA cm^{-2}, FF = 0.63, and η = 5.1 percent. Spectral response measurements indicated an Al content of x = 0.18 based on the location of the long-wavelength cutoff; this value is significantly lower than the x = 0.24 expected on the basis of the deposition parameters, and may represent an advanced indication of problems that had been developing in the TMAl mass-flow controller of the reactor system at the time this cell structure was grown.

During the eleventh month of the program a new group of $Ga_{0.7}Al_{0.3}As$ cell structures was grown by MO-CVD at deposition temperatures in the range 790-800°C. The purpose of those experiments was to provide a comparison of the performance of separate alloy cell structures with the performance of the alloy cells in two-cell SMBSC's. The results of such comparisons could then be used to optimize the growth conditions for the top ($Ga_{1-x}Al_xAs$) cell in the SMBSC's.

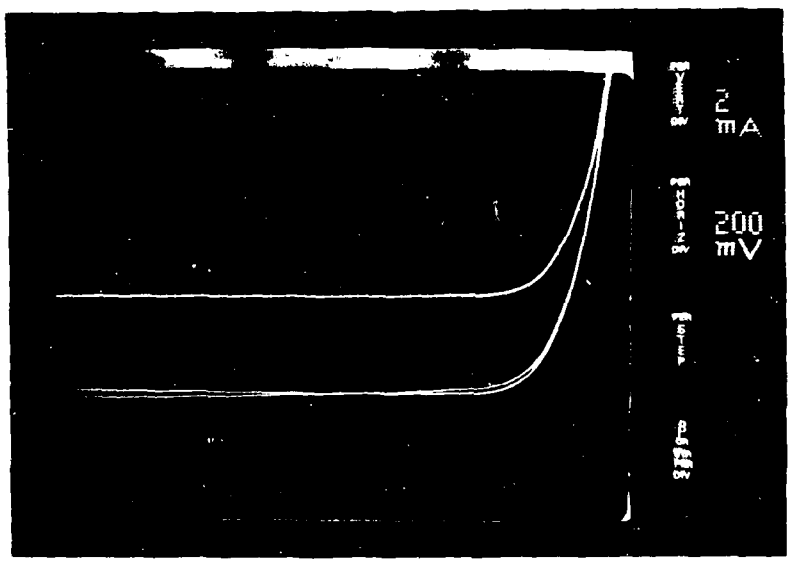


Figure 83. Dark and Illuminated (microscope lamp) I-V Curves for Window-type $Ga_{0.76}Al_{0.24}As$ p-n Junction Solar Cell (0.5cm x 0.5cm) Grown by MO-CVD at ~750°C on (100)GaAs:Te Substrate

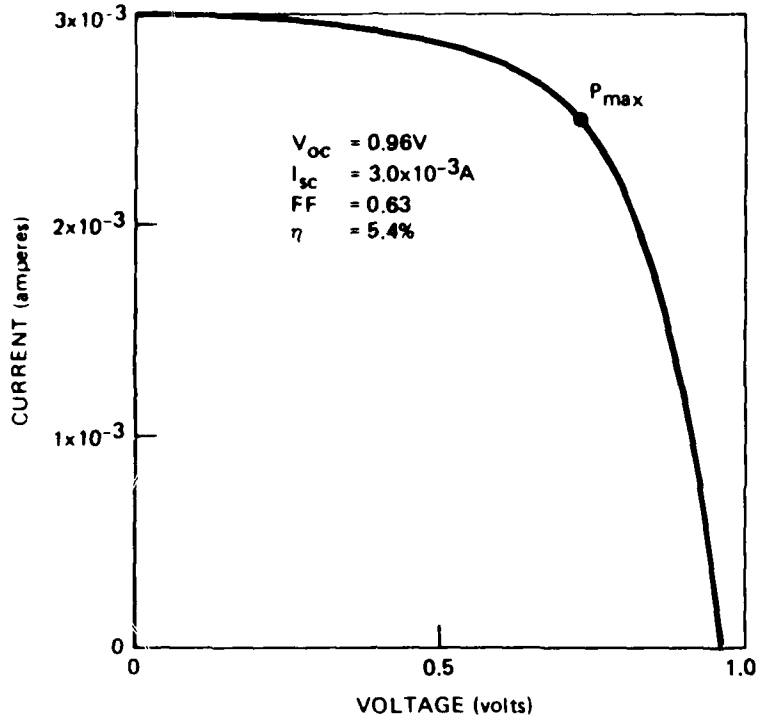


Figure 84. Illuminated I-V Curve (fourth quadrant) of $Ga_{0.76}Al_{0.24}As$ Solar Cell from Same Array as that of Figure 83 but Obtained with AM0 Simulator

One of these cell structures again involved a thin n-type GaAs buffer layer, this time on a substrate of (100)GaAs:Si. The ~1000Å window layer was p-type $Ga_{0.1}Al_{0.9}As$, while the active p and n regions of $Ga_{0.7}Al_{0.3}As$ were ~1.1μm and 4.0μm thick, respectively. No cap layer was used. All layers were deposited at 790°C.

The dark and illuminated I-V curves for one of the 0.5cm x 0.5cm individual cells fabricated in this structure, as obtained with the microscope lamp illumination, are shown in Figure 85. A very soft forward dark characteristic was obtained and – although V_{oc} was ~1V and J_{sc} was ~18mA/cm^2 – the characteristic under illumination exhibited an inflection that may indicate a contact problem, at best. All of the cells on this sample had essentially the same type of I-V characteristics and V_{oc} and J_{sc} values.

In the final two months of Phase 1, after the change in program emphasis had been adopted, considerable effort was devoted to the GaAℓAs cell. Additional cell structures were grown by MO-CVD, and Zn diffusion was used in the processing of some of the alloy cells for the purpose of possibly improving cell performance. Emphasis was on achieving improved understanding and control of the properties of the alloy cell, since it had become evident that the alloy cell had been limiting the performance of the two-cell GaAℓAs-GaAs SMBSC's fabricated prior to that time.

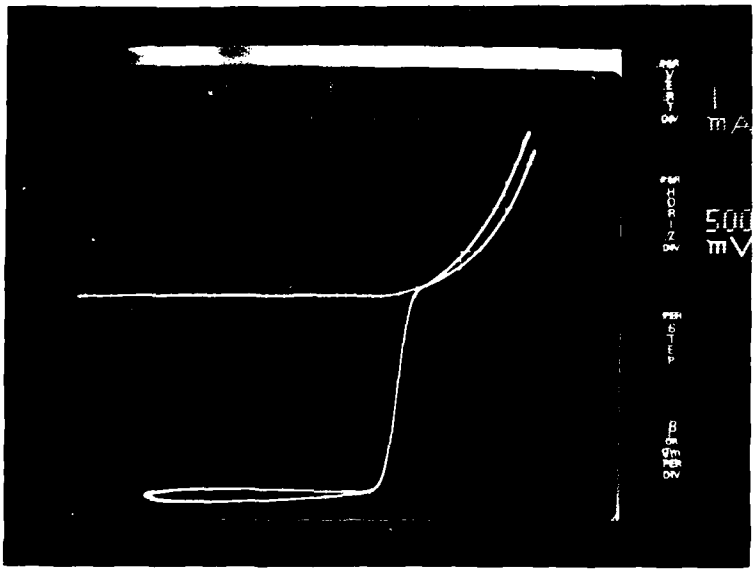


Figure 85. Dark and Illuminated (microscope lamp) I-V Curves for Window-type $Ga_{0.7}Al_{0.3}As$ p-n Junction Solar Cell (0.5cm x 0.5cm) Grown by MO-CVD at ~790°C on (100)GaAs:Si Substrate

Of the several new GaAlAs cell structures grown by MO-CVD, all but one were grown on Si-doped GaAs single-crystal substrates; one cell was grown on a Te-doped substrate, and all were grown at ~750°C. Those grown early in this period had window layers of Al composition x in the 0.80-0.90 range and thicknesses of 0.10 or 0.15μm. The active p layers (Zn-doped) had nominal Al composition x ranging from 0.18 to 0.26, with thicknesses of 1.3 or 1.5μm. Thicknesses of the n-type alloy layer were typically 5.6-6.0μm.

Later in the period, however, a special group of three alloy cells was prepared with all properties common except for the thickness of the active p-type GaAlAs layer, in order to determine experimentally the effect of that critical parameter on cell performance. That group of alloy cells all had window layers of intended composition $Ga_{0.1}Al_{0.9}As$ and thickness in the 600-800Å range, with both junction layers having composition $Ga_{1-x}Al_xAs$ (x 0.20-0.22). The p layer thicknesses were measured to be 1.28, 0.65, and 0.32μm in these three samples. All of these alloy cell structures were processed into devices and characterized with the automated cell testing apparatus.

The alloy cells previously made by MO-CVD, whether separate cells or part of a two-cell SMBSC with GaAs, generally exhibited very low J_{sc} values – typically <5mA/cm^2 for AM0 illumination. Photoresponse measurements had indicated that the electron diffusion lengths in the p layers were probably less than the junction depths, so that relatively poor collection efficiency, especially evident at short wavelengths, had resulted. The group of three alloy cells referred to above was prepared specifically to investigate this problem. Those cells together with the other alloy cells grown and evaluated in the final two months are listed in Table 8, which shows the principal physical parameters of the structures.

Also listed are two other alloy cells grown by MO-CVD earlier in the program, one of which (AB90526A) was characterized in detail with the more recent cells. The other, listed for comparison only, is the alloy cell (AB90427A) discussed earlier and represented in Figures 83 and 84.

The measured photovoltaic properties of the alloy cells listed in Table 8 are given in Table 9, as determined with AM0 simulated illumination (ELH lamp) in the automated facility. The Aℓ content x in the p and n junction-forming layers of $Ga_{1-x}Al_xAs$ of each of the cells was deduced from the location of the long-wavelength cutoff in the measured spectral response curve, based on the published bandgap-composition data of Panish (Ref 13).

The tabulated results show that the open circuit voltage V_{oc} of the cell increases as the Aℓ content of the junction-forming alloy increases. The measured range of variation of V_{oc} with the deduced Aℓ content in the junction layers for these cells is plotted in Figure 86, along with a reference plot (linear) of expected bandgap in the junction region as a function of Aℓ content. The observed increase in V_{oc} with deduced Aℓ content is considerably slower than the linear variation of bandgap with Aℓ content until Aℓ compositions ≥ 0.30 are reached, and the V_{oc} values at all but the lowest Aℓ compositions (i.e., for GaAs rather than GaAℓAs cells) are significantly less than the expected values. In fact, there is relatively little increase in V_{oc} with Aℓ content of the junction layers until x exceeds ~ 0.2. Some of the alloy cells had relatively low short-circuit current densities as a result of junctions that were too deep (i.e., p-type active regions too thick), so the problem of the low V_{oc} values could be reduced somewhat as the alloy cell design is optimized. However, further work is clearly needed in order to improve the V_{oc} values and thus realize the potential peak efficiencies of which these devices should be capable.

The short-circuit current density J_{sc} obtained with these cells depends upon both the Aℓ content and the thickness of both the window layer and the junction layer. The variation of J_{sc} with thickness of the p-type alloy layer (i.e., junction depth) for the group of three cells grown with p layer thicknesses of 1.28, 0.65, and 0.32μm is shown in Figure 87. It appears that increasing the junction depth from ~ 0.3 to ~ 0.7μm had little effect on J_{sc}, but further increase to ~ 1.3μm produced a major reduction in the collected short-circuit current density. This result suggested a minority carrier diffusion length of ~ 0.5μm for this material, indicating that a shallow-junction structure (i.e., ≤0.5μm) is needed for optimized performance for the alloy cell.

Table 8. Principal Physical Parameters of GaAlAs Heteroface Solar Cell Structures Grown by MO-CVD and Processed in Final Two Months of Phase 1

Sample No.	Substrate Material (all (100))	Deposition Temperature (°C)	Nominal Al Concentr. (x) in Window	Nominal Window Thickness (μm)	Nominal Al Concentr. (x) in Junction	Nominal Junction Depth (μm)	Type of Junction Processed	Nominal n Layer Thickness (μm)
AB90427A	GaAs:Te*	~750	0.80	0.1	0.24	0.6	As grown	2.4
AB90526A	GaAs:Te**	~750	0.90	0.1	0.30	1.1	As grown	3.0
AB90809A	GaAs:Si	~750	0.88	0.1	0.26	1.5	As grown	6.0
AB90810A(1)	GaAs:Si	~750	0.90	0.1	0.20	1.3	Zn diffused	5.6
AB90810A(1)	GaAs:Si	~750	0.90	0.1	0.20	1.3	As grown	5.6
AB90810A(2)	GaAs:Si	~750	0.90	0.1	0.20	1.3	As grown	5.6
AB90811A	GaAs:Te	~750	0.80	0.15	0.20	1.3	As grown	5.6
AB90811A	GaAs:Te	~750	0.80	0.15	0.20	1.3	Zn diffused	5.6
AB90813A	GaAs:Si	~750	0.80	0.1	0.18	1.3	As grown	5.6
AB90813A	GaAs:Si	~750	0.80	0.1	0.18	1.3	Zn diffused	5.6
AB90823A	GaAs:Si	~750	0.90	0.1	0.20–0.22	1.28†	As grown	5.0
AB90823B	GaAs:Si	~750	0.90	0.1	0.20–0.22	0.65†	As grown	5.0
AB90824A	GaAs:Si	~750	0.90	0.1	0.20–0.22	0.35†	As grown	5.0

*GaAs n-type buffer layer 0.2 μm thick grown by MO-CVD on GaAs substrate.

**GaAs n-type buffer layer 0.43 μm thick grown by MO-CVD on GaAs substrate.

†Junction depth (p layer thickness) measured in SEM.

Table 9. Measured Photovoltaic Properties of MO-CVD GaAℓAs Heteroface Solar Cells Listed in Table 8 (AM0 simulated illumination).

Sample No.	Type of Junction Processed	Deduced* Aℓ Concentr. (x) in Junction	Nominal Junction Depth (μm)	V_{oc} (volts)	J_{sc} (mA/cm^2)	Fill Factor	Efficiency (%)
AB90427A	As grown	0.18	0.6	0.963	12.04	0.628	5.4
AB90526A	As grown	0.25	1.1	0.997	1.28	0.616	0.59
AB90809A	As grown	0.38	1.5	1.017	1.50	0.733	0.82
AB90810A(1)	Zn diffused	0.33	1.3	1.147	4.49	0.741	2.83
AB90810A(1)	As grown	0.33	1.3	1.081	2.74	0.722	1.59
AB90810A(2)	As grown	0.33	1.3	1.178	3.05	0.745	1.99
AB90811A	As grown	0.27	1.3	1.131	3.48	0.748	2.18
AB90811A	Zn diffused	0.27	1.3	1.129	4.05	0.745	2.53
AB90813A	As grown	0.21	1.3	1.031	3.18	0.763	1.85
AB90813A	Zn diffused	0.21	1.3	1.034	3.75	0.762	2.19
AB90823A	As grown	0.20	1.28**	0.969	1.44	0.772	0.80
AB90823B	As grown	0.21	0.65**	1.046	6.56	0.765	3.90
AB90824A	As grown	0.21	0.35**	1.018	6.62	0.760	3.79

*Aℓ content of junction layers deduced from long-wavelength cutoff in measured spectral response curve.

**Junction depth (p layer thickness) measured in SEM.

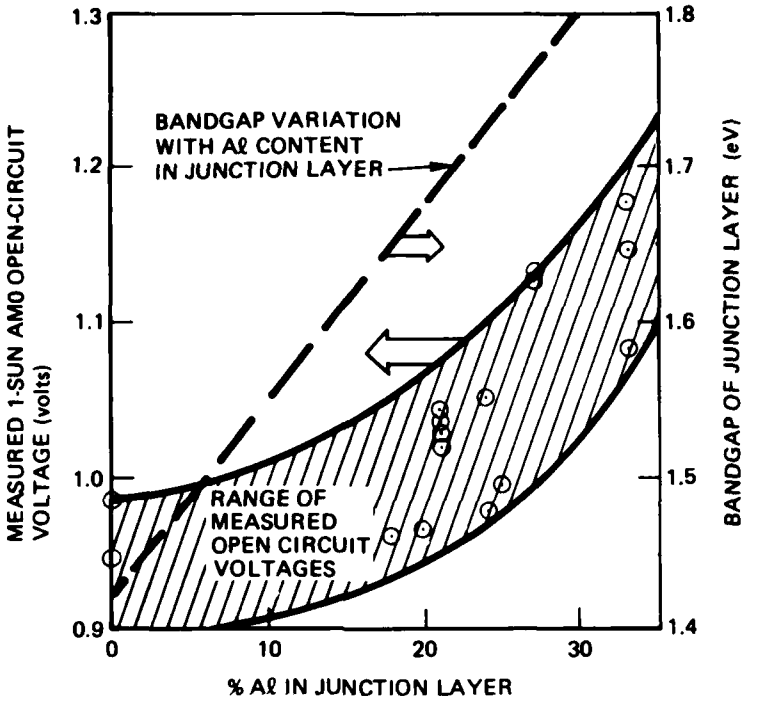


Figure 86. Measured V_{oc} Values for MO-CVD Alloy Cells of Tables 8 and 9 as Function of Deduced Aℓ Content of Junction-forming Layers, for Simulated AM0 Illumination. Variation of Expected Bandgap Energy with Aℓ Content also Shown, for Reference

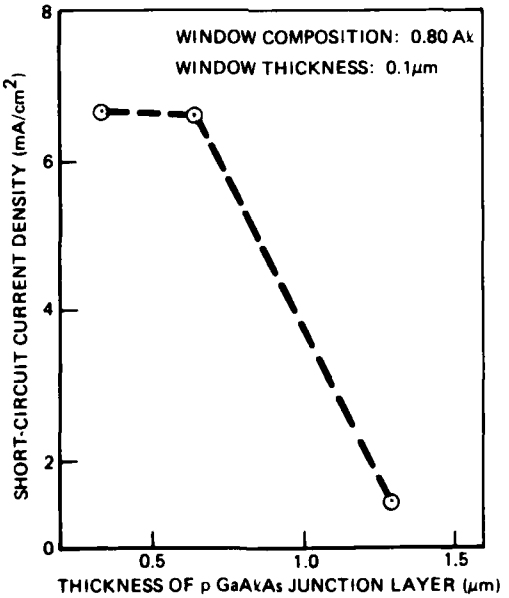


Figure 87. Dependence of J_{sc} upon Junction Depth (p layer thickness) for Three $Ga_{0.8}Al_{0.2}As$ Solar Cells Made by MO-CVD, for Simulated AM0 Illumination (See Tables 8 and 9)

The spectral response curves for these same three cells are given in Figure 88, and the results show that better blue response is realized for shallower junctions, as would be expected. However, the total J_{sc} values for the two cells with junction depths of ~0.7 and ~0.3μm are nearly the same, as indicated in Figure 87. because the enhanced blue response for the ~0.3μm junction depth is approximately compensated by the reduced red response, as shown in Figure 88.

The effect of window layer composition on cell properties is indicated by the two sets of spectral response curves of Figure 89. The cell structure with a window layer of nominal composition $Ga_{0.1}Al_{0.9}As$ (sample AB90810A(1), Tables 8 and 9) exhibits a stronger blue response and larger short-circuit current density (larger area under the response curve) than does a cell structure (sample AB90813A, Tables 8 and 9) with a nominal window layer composition of $Ga_{0.2}Al_{0.8}As$. This difference is seen to hold even though the Al content of the junction layers is higher in the structure of sample AB90810A(1).

The use of Zn diffusion during the processing of some of the alloy structures into completed solar cells was also pursued during this period. The purpose of the Zn diffusion was to form a highly conductive window layer and a front-surface field and thus possibly to improve the performance of the cell. For the MO-CVD cells so treated there was a higher short-circuit current density than for cells made from the same deposited sample but without the Zn diffusion. (See samples AB90810A(1), AB90811A, and AB90813A, Table 9.) This effect is also shown in Figure 89 for two of the sets of cells, for which a significantly higher total photocurrent response is evident for the Zn-diffused cells than for the untreated (as-grown) cells. However, for earlier alloy cells processed with Zn diffusion and for the LPE-grown alloy cells described in Section 2.5.1 the use of Zn appeared to cause a decrease in the short-circuit current density. The reasons for the difference are not known.

On the basis of all of the above results, growth of another group of alloy cells was undertaken just prior to the end of Phase 1, for the purpose of achieving cell parameters that would result in significantly improved GaAlAs cells. Thus, a shallow junction (<0.5μm) in an active region of composition $Ga_{0.7}Al_{0.3}As$ and a window layer of composition $Ga_{0.10}Al_{0.90}As$ and thickness ~800Å were the parameter goals. It was found, however, that p layer thicknesses achieved were closer to 0.8μm and window layer thicknesses were ~1200Å in the alloy cells, whether grown separately or as part of a stacked cell assembly.

Consequently, although analysis of these latest alloy cells was not complete at the conclusion of Phase 1, it appeared that cell performance was considerably poorer than expected. Work on improving the properties of the alloy cells is expected to continue into the Phase 2 program.

2.4.2 Connecting Junctions in GaAs and GaAlAs

The extensive efforts devoted to achieving conducting junctions in GaAs for the purpose of providing intercell connections in GaAs-Ge and/or GaAlAs-GaAs two-cell SMBSC structures in the Phase 1 program were described in Sections 2.2.4.1 and 2.2.4.2.

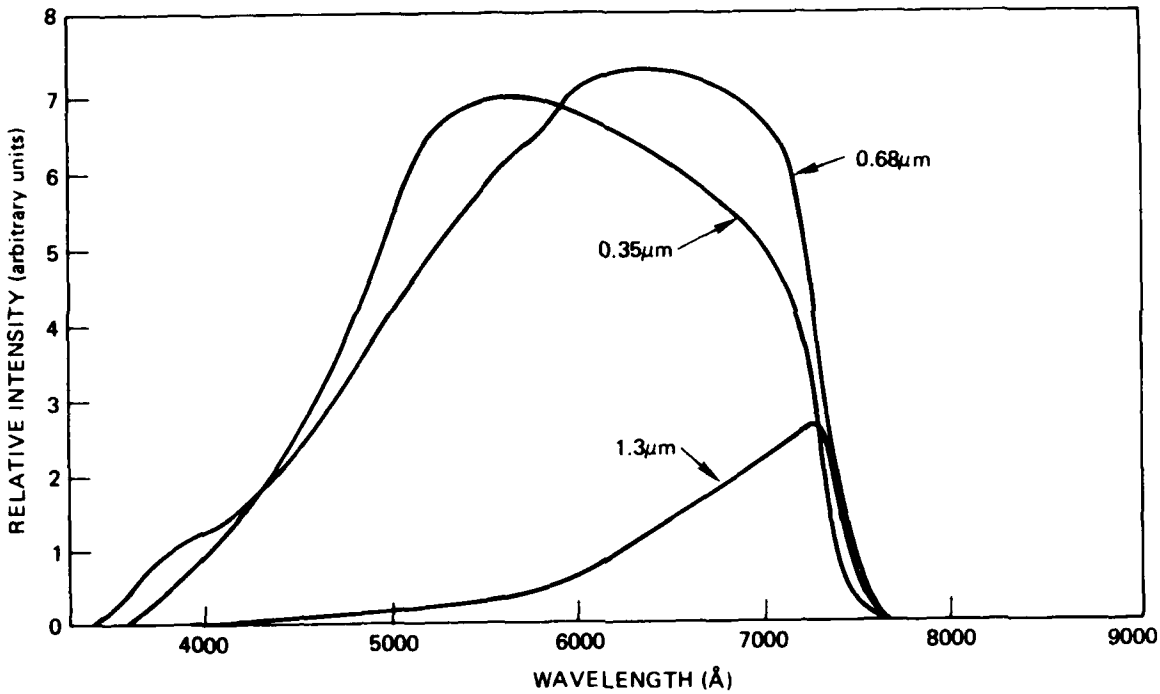


Figure 88. Spectral Response Curves for Three MO-CVD $Ga_{0.8}Al_{0.2}As$ Cells of Different Junction Depths (p layer thickness).
(See Tables 8 and 9 and Figure 87)

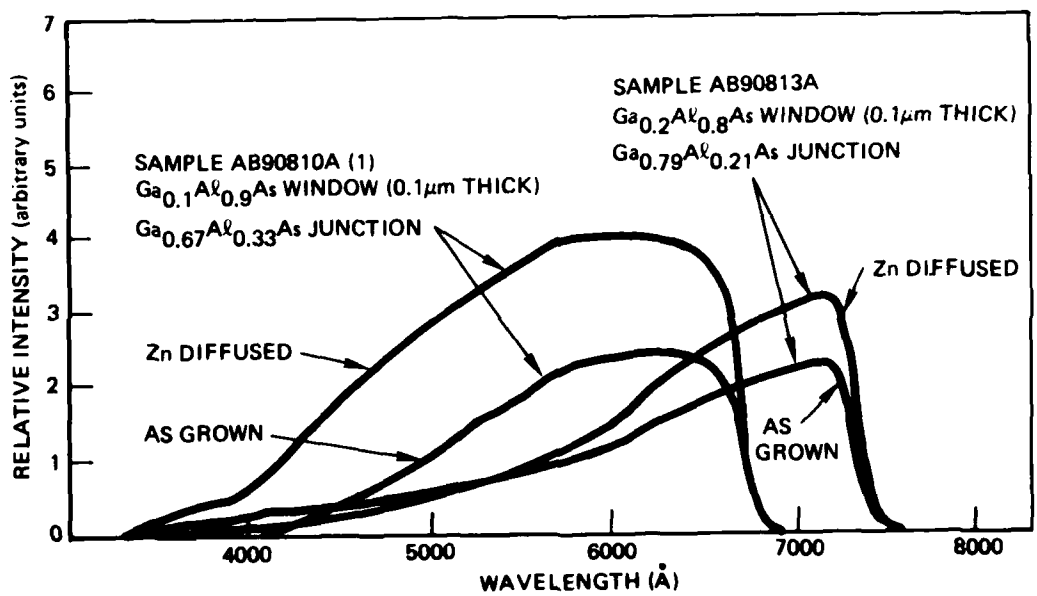


Figure 89. Spectral Photoresponse Curves for GaAlAs Solar Cells Made in MO-CVD Structures Having Different GaAlAs Window-layer Compositions (and different junction-layer compositions), Processed Both in As-grown Condition and with Zn Diffusion

Consequently, the discussion in this section is confined to a description of the efforts to achieve tunneling junctions in GaAℓAs, for use in connecting GaAℓAs and GaAs cells in two- or three-cell SMBSC structures.

The first GaAℓAs junction structures grown with doping concentrations intended to produce tunneling characteristics were prepared in the third and fourth months of the program. Several n^+/p^+ $Ga_{1-x}Al_xAs$ structures with $x \approx 0.37$ were deposited by MO-CVD on GaAs substrates at ~750°C. None of those first structures grown in this configuration exhibited tunneling properties, however.

Evaluation of the properties of the first few unsuccessful structures provided the information needed to identify deposition conditions that did result in tunneling properties. The experiments with GaAs tunneling junctions (Section 2.2.4.1) had shown that lower deposition temperatures than those normally used for GaAs film growth by the MO-CVD process were required for achieving tunneling characteristics. Consequently, single layers of GaAℓAs alloys were grown on GaAs substrates at ~700°C to establish alloy compositions of layers grown under selected conditions. The alloy composition was determined by x-ray double-crystal diffractometer measurements and – for alloy films with compositions in the direct-bandgap range – by room-temperature photoluminescence measurements. It was found that alloy composition is not strongly dependent upon deposition temperature for a given set of other parameters in this range. That is, the dependence of the x value on the TMAℓ:TMG partial-pressure ratio during film growth agreed well with that determined in earlier studies using different deposition conditions (especially temperature).

During the eighth month of the program a $Ga_{0.92}Al_{0.08}As$ p^+ n^- epitaxial structure was grown by MO-CVD at 700°C on a GaAs:Si substrate, as the next step in identifying the deposition conditions required for producing a tunnel diode structure in this material. Preliminary evaluation of this sample using In contacts and the mechanical probe indicated a weak tunneling characteristic. However, when individual mesa diodes were fabricated with ohmic contacts the evaluation showed a heavily doped back-to-back diode characteristic but no tunneling behavior.

Despite this unsuccessful result, two-cell SMBSC structures each consisting of a $Ga_{0.6}Al_{0.4}As$ p-n junction cell and a GaAs p-n junction cell grown sequentially on a GaAs:Te substrate, with the two cells connected by an n^+/p^+ junction structure, were grown entirely by the MO-CVD process. One such SMBSC structure had the n^+/p^+ junction in the GaAs (see Section 2.2.4.1), and the other had the n^+/p^+ junction in an alloy double layer of composition $Ga_{0.92}Al_{0.08}As$. The configuration of this structure was as shown schematically in Figure 90.

Characterization of the resulting structure, as described in Section 2.4.3, indicated that the junction did not have tunneling properties, despite the fact that the doping concentrations on both sides of the junction were believed to be very high.

The lack of clear-cut success in achieving good tunneling properties in n^+ p^+ junction structures in GaAℓAs resulted in attention being shifted to the formation of the required connecting junction structures in GaAs, for which success had

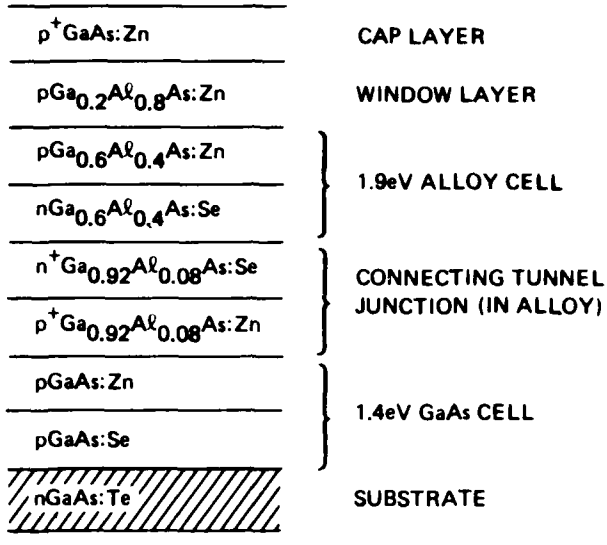


Figure 90. Configuration of Two-cell SMBSC Grown by MO-CVD on GaAs Single-crystal Substrate, with Connecting Junction in GaAℓAs

been achieved relatively early in the Phase 1 program (see Section 2.2.4.1). Because of the preference for having the connecting junction in the alloy rather than in the GaAs, however, it is expected that further attention will be given to the GaAℓAs alloys for this purpose in the Phase 2 program.

2.4.3 GaAℓAs-GaAs Two-cell SMBSC's

The problems involved in joining cells in the GaAℓAs-GaAs materials system to make two-cell (or three-cell) SMBSC structures were first investigated all at one time in the eighth month of the program, at which time complete two-cell GaAℓAs-GaAs SMBSC structures were prepared entirely by MO-CVD techniques. The structures consisted of a GaAs p-n junction cell, an n+-p+ connecting junction structure, and a GaAℓAs p-n junction cell grown in that sequence on a GaAs:Te single-crystal substrate. One of the structures had the connecting junction in GaAs and the other had the connecting junction in GaAℓAs (see Figure 90). In both cases the alloy cell had the composition $Ga_{0.6}Al_{0.4}As$, with a window layer of $Ga_{0.2}Al_{0.8}As$. The GaAs cells in both cases were without window layers.

Both structures were processed into 0.5cm x 0.5cm cells in the usual way and were tested with the microscope lamp and probe contact. The I-V curves were obtained both before and after removal of the top p^+GaAs cap layer (by etching).

Typical I-V curves for two of these SMBSC assemblies are shown in Figures 91 and 92. The two-cell device represented in Figure 91 had the connecting n^+-p^+ junction in the $Ga_{0.92}Al_{0.08}As$ *double* layer, as shown in the schematic diagram of Figure 90. Apparently this junction did not have a tunnel-diode characteristic, despite the fact that the doping *concentrations were* designed for that purpose. As a result, both the I_{sc} and the V_{oc} values were low and the curve shape unacceptable.

The I-V characteristics for the other two-cell structure, in this case with the connecting n^+-p^+ junction in a GaAs double layer, are represented in Figure 92. The dark I-V curve for this device appears to be good, but the response under illumination by the microscope lamp again appears to be severely limited by the properties of the connecting junction. That is more apparent in Figure 93, which shows the dark and illuminated reverse I-V characteristics of this same cell. The data show that the I_{sc} of this cell was limited by the nonlinear I-V characteristic of the connecting n^+-p^+ junction in the GaAs. Once this junction became conducting the cell current increased rapidly to a value of ~5mA.

Soon thereafter, additional GaAlAs-GaAs two-cell SMBSC structures were grown by MO-CVD with properties somewhat different from those of the first structures described above. These structures were again processed into 0.5cm x 0.5cm individual cells and tested for photoresponse with the microscope lamp illumination.

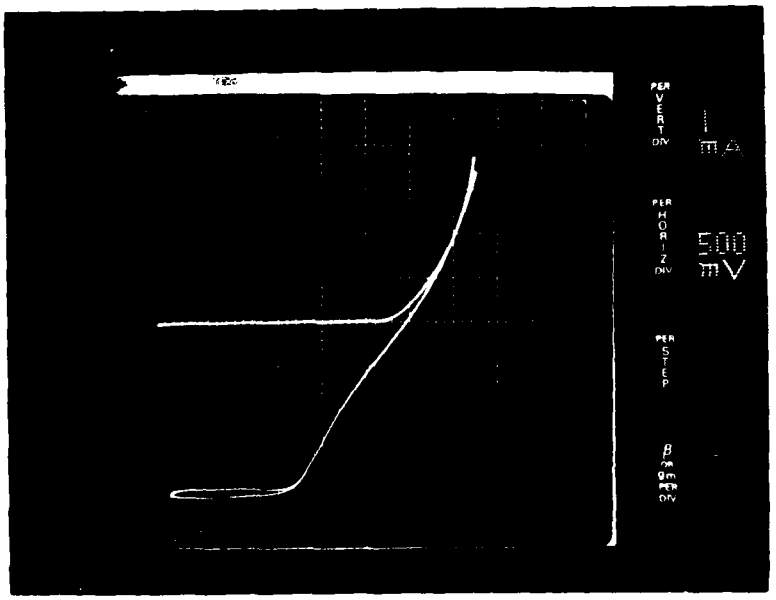


Figure 91. Dark and Illuminated (microscope lamp) I-V Characteristics of Two-cell SMBSC Grown by MO-CVD, with $Ga_{0.6}Al_{0.4}As$ Cell and GaAs Cell Connected by Intermediate n^+-p^+ Junction in $Ga_{0.92}Al_{0.08}As$

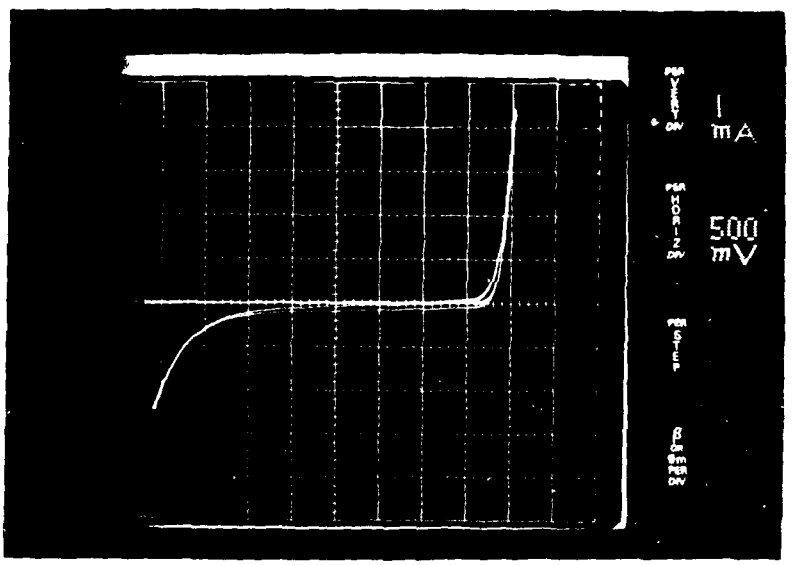


Figure 92. Dark and Illuminated (microscope lamp) I-V Characteristics of Two-cell SMBSC Grown by MO-CVD, with $Ga_{0.6}Al_{0.4}As$ Cell and GaAs Cell Connected by Intermediate n^+-p^+ Junction in GaAs

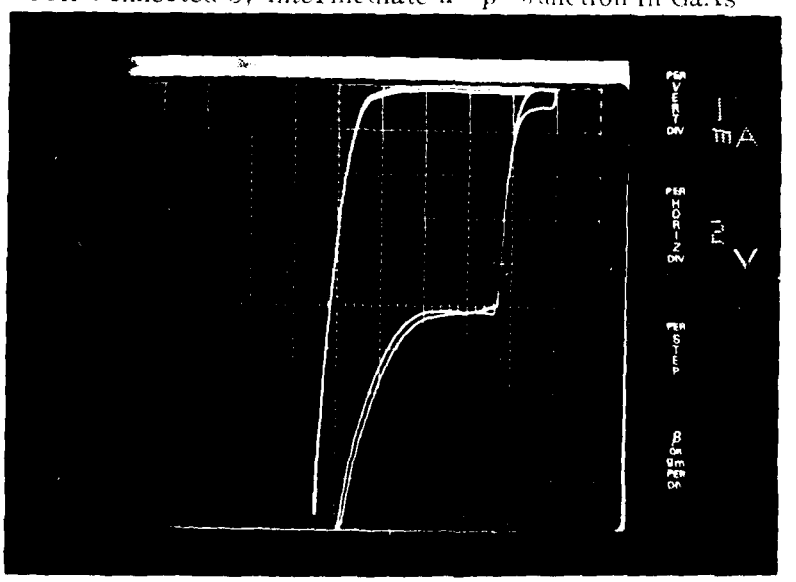


Figure 93. Dark and Illuminated (microscope lamp) Reverse I-V Characteristics of Two-cell $Ga_{0.6}Al_{0.4}As$-GaAs SMBSC Represented in Figure 92

Cells from the best of these samples showed V_{oc} values of ~2.1V and I_{sc} values of ~1.1mA under this illumination. This particular sample had the structure shown schematically in Figure 94. The growth temperatures of the various regions of this cell structure were as follows: 1) GaAs cell and $Ga_{0.7}Al_{0.3}As$ window layer, ~700°C; 2) GaAs n+/p+ connecting junction layers, ~630°C; 3) $Ga_{0.7}Al_{0.3}As$ cell and $Ga_{0.2}Al_{0.8}As$ window layer, ~750°C.

A typical set of I-V characteristics for one of the cells on this sample, as obtained with the microscope lamp, is shown in Figure 95. It is evident from the curves that this structure represents the first successful achievement of a stacked or tandem cell grown completely by a vapor-phase process. The open-circuit voltage shown is believed to be the highest achieved up to that time for a tandem cell grown by any process. These major accomplishments provided the necessary evidence that the goals of this program can be achieved by the MO-CVD technique.

The response of the $Ga_{0.7}Al_{0.3}As$ cell in the above structure probably limited the response of the stacked assembly. The performance of the particular cell assembly represented in Figure 95 was probably below what could have been realized because the $Ga_{0.2}Al_{0.8}As$ window layer was inadvertently removed during processing and the wafer was subsequently reprocessed. Photoresist lift-off problems then occurred as a result of the rework requirement. Consequently, the cell performance was probably poorer than it would have been had this not occurred.

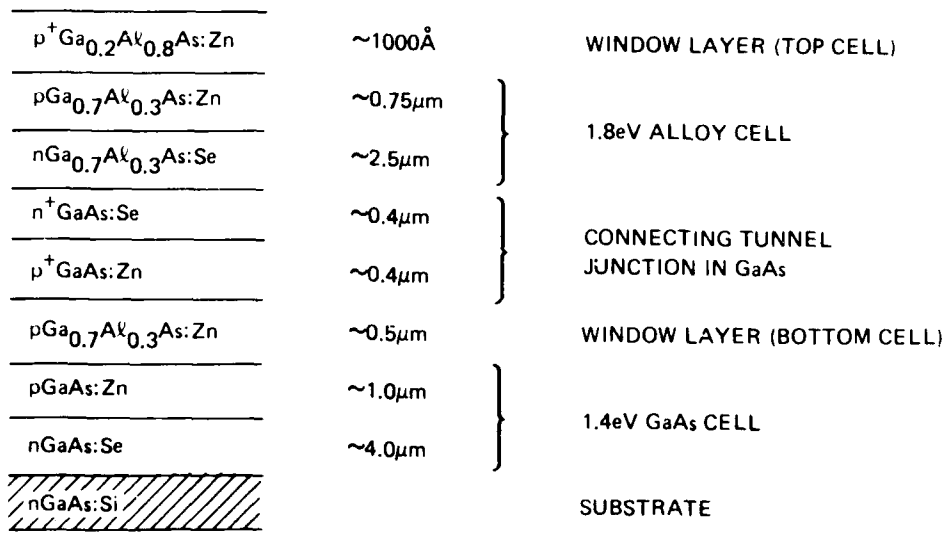


Figure 94. Configuration of Two-cell GaAlAs-GaAs SMBSC for which Voltage Addition was Observed under Illumination

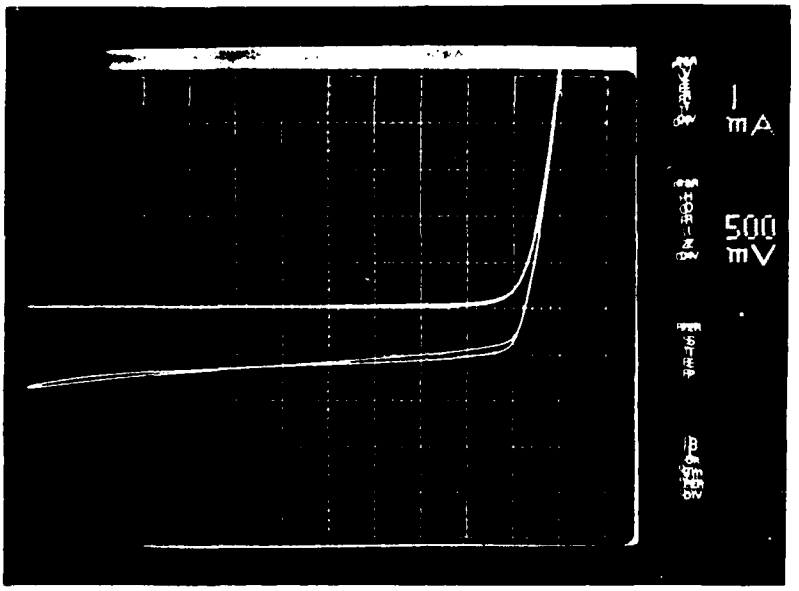


Figure 95. Dark and Illuminated (microscope lamp) I-V Curves for Two-cell SMBSC Grown Entirely by MO-CVD on GaAs:Si Substrate, with $Ga_{0.7}Al_{0.3}As$ Cell and GaAs Cell Connected by Intermediate n^+-p^+ Junction in GaAs.

Additional two-cell GaAlAs-GaAs SMBSC structures were grown in the following month, with slightly modified dimensional parameters as shown in Figure 96. Layers 1-3 were typically deposited in the 700-750°C range; layers 4 and 5 were deposited at ~630°C; layers 6-8 were grown at ~750°C. As before, the composites were processed into arrays of 0.5cm x 0.5cm cells. The p-layer contact metallization was applied directly to the $Ga_{0.7}Al_{0.3}As$:Zn layer (layer 7) of the alloy cell.

I-V curves obtained with the microscope lamp for one of the two-cell SMBSCs on one of the wafers are shown in Figure 97. The V value is again seen to be ~2.1V, indicating that the individual cell voltages are indeed adding. This cell, however, had a short-circuit current of only about 0.85mA for the illumination conditions employed, compared with ~1.1mA for the cell shown in Figure 95.

Again it is believed that the SMBSC current was being limited by the current produced in the alloy (top) cell. The "kink" observed in the dark I-V curve is not understood, but it could have been the result of a leaky p-n junction in the top cell (i.e., in the $Ga_{0.7}Al_{0.3}As$ cell).

8	$p^+Ga_{0.2}Al_{0.8}As:Zn$	~1000Å	$Ga_{1-x}Al_xAs$ CELL (1.8eV)
7	$pGa_{0.7}Al_{0.3}As:Zn$	~0.9μm	
6	$nGa_{0.7}Al_{0.3}As:Se$	~3.0μm	
5	$n^+GaAs:Se$	~0.4μm	CONNECTING JUNCTION
4	$p^+GaAs:Zn$	~0.4μm	
3	$pGa_{0.7}Al_{0.3}As:Zn$	~0.3μm	GaAs CELL (1.4eV)
2	pGaAs:Zn	~1.0μm	
1	nGaAs:Se	~4.0μm	
	nGaAs:Si		(100)-ORIENTED SUBSTRATE

Figure 96. Modified Configuration of Two-cell GaAlAs-GaAs SMBSC Structure Grown by MO-CVD

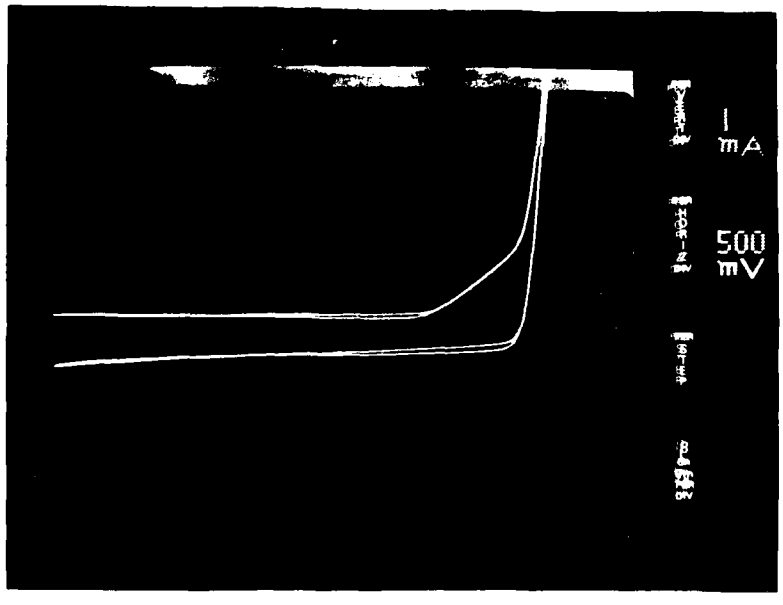


Figure 97. Dark and Illuminated (microscope lamp) I-V Curves for Two-cell SMBSC Grown Entirely by MO-CVD on GaAs:Si Substrate, with $Ga_{0.7}Al_{0.3}As$ Cell on Top and GaAs Cell on Bottom Connected by Conducting n^+-p^+ Junction in GaAs Intermediate Layer

Additional two cell SMBSC structures were grown subsequently using slightly modified parameters to attempt to improve the current response of the alloy cell. These samples were processed into arrays of 0.5cm x 0.5cm solar cells using the fabrication techniques described earlier. Some of these structures had the n^+ p^+ GaAs connecting junction grown at ~710°C (rather than ~630°C as in previous structures) and the $Ga_{0.7}Al_{0.3}As$ top cell grown at ~775°C (rather than ~750°C). While these cells showed relatively good values of photocurrent under reverse bias conditions, the values of I_{sc} and V_{oc} were not good because of large leakage currents, probably in the $Ga_{0.7}Al_{0.3}As$ cells. This is shown in the I-V curves of Figure 98.

Some of the new SMBSC structures were grown with the configuration shown in Figure 99, which involves slightly changed dimensions of some of the layers of the device. Deposition temperatures employed were ~700°C for the bottom GaAs cell and its $Ga_{0.7}Al_{0.3}As$ window layer, ~630°C for the layers of the GaAs n^+ p^+ connecting tunnel junction, and both 750°C and 800°C for the top alloy cell and its window layer.

These structures were processed into cell arrays by the usual procedures, and individual 0.5cm x 0.5cm cells were characterized using the microscope lamp illumination and the mechanical probe contacts. Dark and illuminated I-V curves for a typical individual SMBSC from one of these wafers, in which the alloy cell was grown at ~800°C, are shown in Figure 100. While the usual "reference"

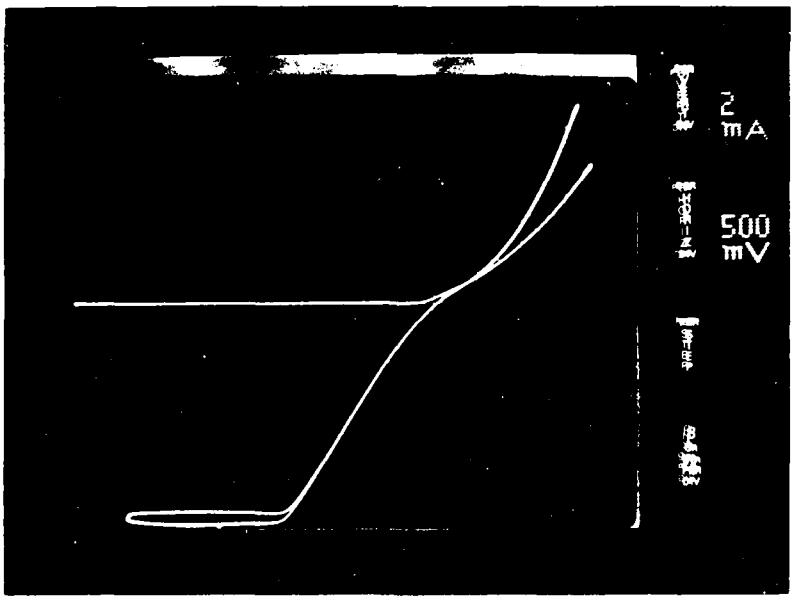


Figure 98. Dark and Illuminated (microscope lamp) I-V Curves for Two-cell SMBSC (0.5cm x 0.5cm) Grown by MO-CVD on GaAs:Si Substrate, with $Ga_{0.7}Al_{0.3}As$ Cell on Top (grown at ~775°C) and GaAs Cell on Bottom, Connected by n^+ p^+ Conducting Junction in GaAs Intermediate Layer Grown at ~710°C

$p^+Ga_{0.2}Al_{0.8}As$:Zn	~1000Å		TOP CELL WINDOW LAYER
$pGa_{0.7}Al_{0.3}As$:Zn	~0.75μm	}	$Ga_{0.7}Al_{0.3}As$ CELL (1.8eV)
$nGa_{0.7}Al_{0.3}As$:Se	~2.5μm	}	
n^+GaAs:Se	~0.4μm	}	CONNECTING (TUNNEL) JUNCTION
p^+GaAs:Zn	~0.4μm	}	
$pGa_{0.7}Al_{0.3}As$:Zn	~0.5μm		BOTTOM CELL WINDOW LAYER
pGaAs:Zn	~1.0μm	}	GaAs CELL (1.4eV)
nGaAs:Se	~4.0μm	}	
nGaAs:Si	~10 MILS		(100)-ORIENTED SUBSTRATE

Figure 99. Configuration of Two-cell GaAlAs-GaAs SMBSC Used to Produce Photoresponse of Figure 100

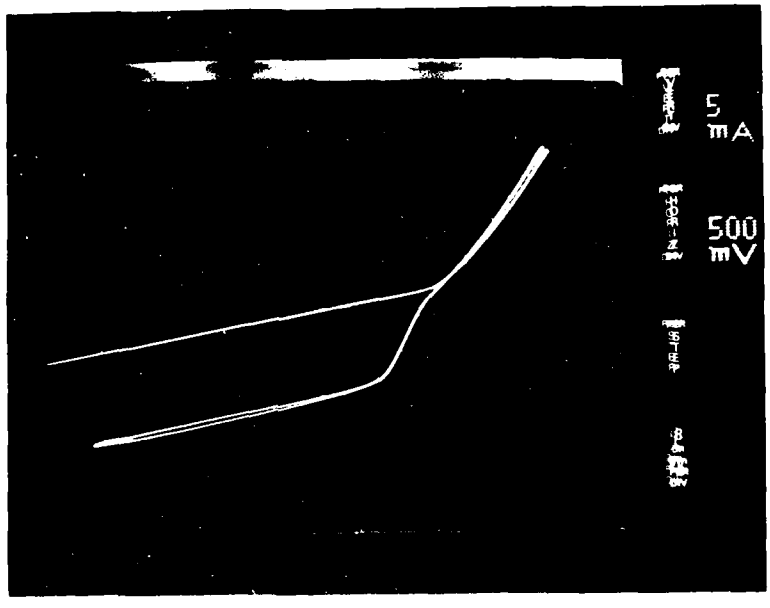


Figure 100. Dark and Illuminated (microscope lamp) I-V Curves for Two-cell SMBSC Grown by MO-CVD on GaAs:Si Substrate, with $Ga_{0.7}Al_{0.3}As$ Alloy Cell on Top and GaAs Cell on Bottom Connected by Connecting n$^+$-p$^+$ Junction in GaAs [illegible] Layer

short-circuit current of 10mA was obtained, the I-V curve shows there was a large leakage current and a relatively low V_{oc} value of ~1.05V, compared with ~2.1V obtained in several previous two-cell SMBSCs.

This may have been the result of dopant diffusion during the growth of the top alloy cell, but further investigation would be required to determine if that were actually the case. Previous studies of the growth of separate $Ga_{0.7}Al_{0.3}As$ alloy cells showed that deposition at ~800°C can lead to somewhat improved performance in this cell. Thus, it may be found desirable to grow the top cell in this SMBSC structure at the higher temperature.

Following the extensive study of the properties of the GaAlAs alloy cells, near the end of the Phase 1 program, an attempt was made to utilize the findings of that study (Section 2.4.1) and prepare two-cell GaAlAs-GaAs SMBSC structures that might exhibit significantly improved properties. A pair of such structures was grown simultaneously in the final month of Phase 1 using (100) GaAs:Si substrates from two different suppliers. The structure configuration that was prepared is shown in Figure 101.

Deposition temperatures were ~750°C for both of the individual cell structures and ~630°C for the GaAs tunnel junction double layer. Both samples were processed into arrays of 1.6mm x 1.6mm cells, and characterization of the cells using the AM0 simulator was begun.

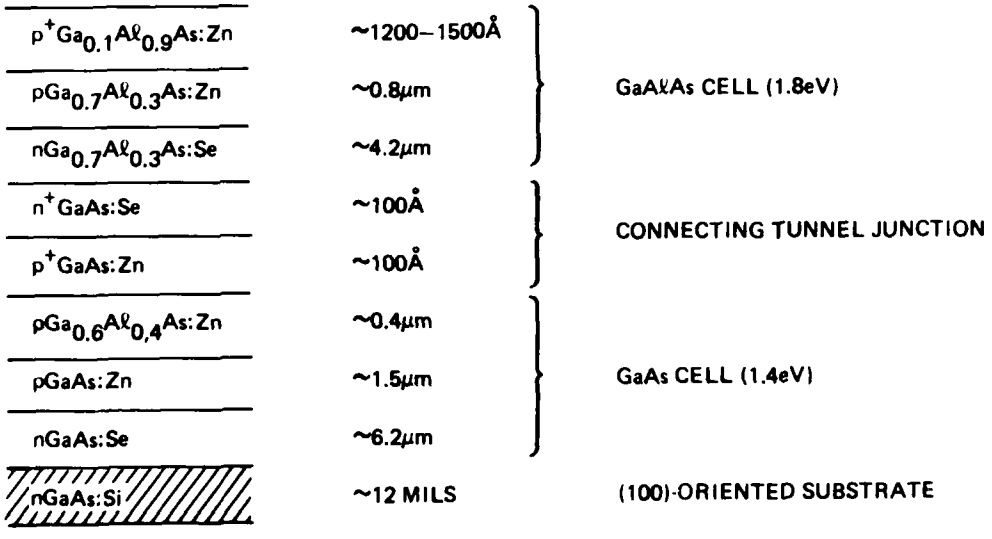


Figure 101. Modified Two-cell GaAlAs-GaAs SMBSC Configuration Designed to Give Improved Performance

Although evaluation of these cells was not completed before the end of Phase 1, initial tests showed disappointing results such as that given in Figure 102, which represents the illuminated I-V curve for one of the individual SMBSC's on the GaAs substrate material obtained from Morgan Semiconductor. Although voltage addition was clearly achieved, the magnitude of V_{oc} shows that either or both of the individual cells were far below the usual quality previously achieved. The very low J_{sc} value also indicates that there may have been problems with the connecting n^+/p^+ GaAs junction, which had been made with layers considerably thinner than those used in previous SMBSC structures of this type. Evaluation of these cells will be continued into Phase 2 to attempt to identify the cause of the poor performance.

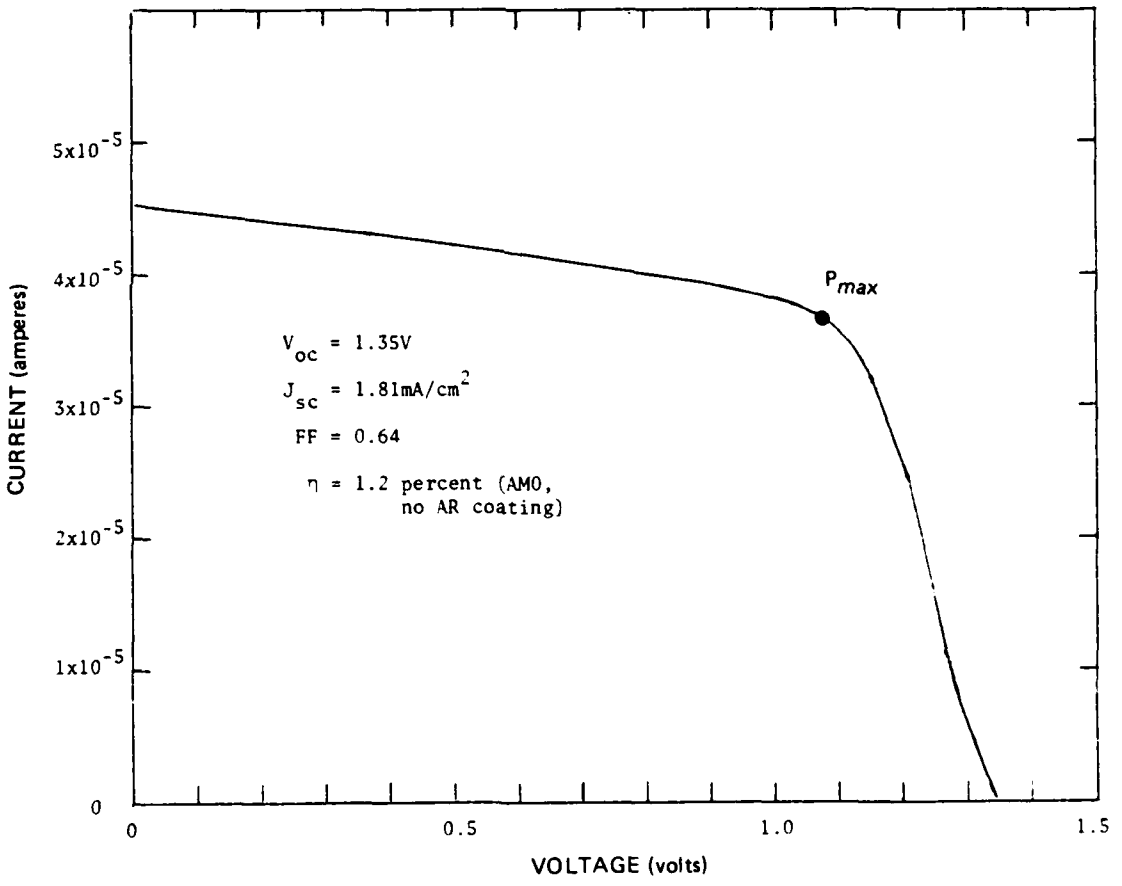


Figure 102. Fourth Quadrant Illuminated (AM0 simulator) I-V Curve for Two-cell SMBSC Made by MO-CVD, Consisting of GaAlAs Cell on GaAs Tunnel Junction on GaAs Cell, All on (100)-oriented GaAs:Si Substrate

2.5 GaAlAs - GaAs - InGaAsP SMBSC TECHNOLOGY DEVELOPMENT

This task was to be carried out mainly at ERC Thousand Oaks, with the three-cell SMBSC to be grown by LPE techniques. GaAs was to be used as the single-crystal substrate, and InP as the window material for the InGaAsP cell, which is an extension of the InGaAs cell to be developed as part of the two-cell SMBSC assembly in Task 3 (Section 2.3).

Although much of the work of this task was to be built upon the work of Task 3, certain aspects of the work were to begin at the start of the contract. The materials and photovoltaic device properties of both the 2.0eV GaAlAs cell and the 1.0eV InGaAsP cell made by LPE were to be studied in detail and characterized.

Near the start of the program the LPE growth of both n^+ and p^+ layers of GaAlAs on p^+GaAs substrates was to be carried out so that electrical conduction of n^+-p^+ junctions in GaAlAs could be investigated. Growth parameters required for obtaining low-resistance conducting (tunneling) interfaces with good growth morphology at the layer surfaces were to be established.

At the same time, the growth of appropriately doped p- and n-type layers of GaAlAs in the proper composition for achieving a 2.0eV p/n LPE cell on an n^+GaAs substrate was to be undertaken, employing an ultrathin p^+GaAlAs surface layer. The photovoltaic properties of this 2.0eV cell structure were to be evaluated and the layer growth conditions adjusted as required to obtain optimum cell properties.

When that goal was successfully achieved the GaAlAs 2.0eV cell technology was to be combined with existing conventional LPE GaAs cell technology. Starting with the n^+GaAs single-crystal substrate, the GaAs heteroface cell structure (consisting of a p-type GaAlAs window layer on a p/n GaAs junction composite) was to be grown on the substrate, followed by an n^+/p^+ GaAlAs tunneling-junction double layer. On that would then be grown the GaAlAs 2.0eV p/n cell structure described above, to complete a two-cell composite. The photovoltaic properties of this two-cell LPE-grown SMBSC system were then to be fully evaluated (Task 6), and the combined photovoltaic performance improved as much as possible by adjusting growth parameters and procedures.

Attention was then to be directed to development of the 1.0eV cell material InGaAsP. Single-crystal substrates of p^+InP were to be used for LPE growth of an inverted heteroface cell structure of n/p InGaAsP, the photovoltaic properties of which would be evaluated so that the growth parameters could be modified if necessary to produce satisfactory cell performance. When that was accomplished the expensive p^+InP substrate would be replaced by the p^+InP/n^+GaAs epitaxial composite grown by LPE on a single-crystal n^+GaAs substrate in the early portion of the work of Task 3, and the same inverted n/p InGaAsP cell structure was to be grown on that composite. The photovoltaic properties of the 1.0eV cell would again be evaluated, and growth conditions further modified to optimize the cell performance if necessary.

This technology for the 1.0eV cell was then to be combined with that already developed (early in the program in this task) for preparing a two-cell structure involving the GaAs cell and the GaAlAs cell connected through a tunneling interface, to produce an integrated procedure for growing a complete three-cell SMBSC by LPE techniques. Growth would be carried out on both sides of an n^+GaAs substrate to achieve the required structure.

As with the component structures, the complete SMBSC structure was to be studied and evaluated in detail; the photovoltaic properties of the complete three-cell assembly were to be determined and compared with the corresponding properties of the individual component cells. Details of the overall fabrication process, including growth sequence, individual layer compositions and impurity concentrations, deposition parameters and cooling schedules, and contact materials and methods of application were to be carefully examined. Modifications indicated for achieving improved overall SMBSC performance would then be made to whatever extent possible.

As in Task 4, InGaP was to be considered as a possible alternative 2.0eV cell material in this task, also, but grown by LPE techniques in this case. The effort, if pursued, would be at a lower level than the primary activity, as was to be the case for the study of this material grown by MO-CVD in Task 4. It was intended that such an investigation of LPE InGaP would be carried through the same stepwise sequence of investigations as that described above for GaAlAs with sufficient thoroughness that a substitution could be made if difficulties of an unresolvable nature were to be encountered in developing the LPE GaAlAs 2.0eV cell.

The possibility of using MBE techniques to form the nonrectifying connecting junctions between cells of the SMBSC structures being investigated in this task was examined relatively early in the program. As indicated in the earlier discussion of GaAs junctions (Section 2.2.4), that method was successfully applied for that purpose as part of the activity of this task.

However, at the time the decision was made to change the program emphasis late in Phase 1 it was determined that the particular three-cell SMBSC that was the goal of this task would not be further pursued in the Phase 1 program. It was also agreed that LPE growth techniques would not be further developed as part of the primary program activity, but that LPE methods would be used as backup or – in certain special cases – in conjunction with CVD or MBE techniques if it appeared that doing so would improve the chances of achieving the program goals.

The investigations carried out on this task during the Phase 1 program are summarized in the following sections.

2.5.1 LPE Growth of GaAlAs on GaAs Substrates

Early in the program some preliminary LPE growth experiments were carried out to prepare alloy layers with the approximate composition $Ga_{0.7}Al_{0.3}As$ on p^+GaAs single-crystal substrates. A complete window-type solar cell structure, such as that required for the 2.0eV cell of the three-cell SMBSC, was grown on an

n^+GaAs substrate. This structure consisted of a $Ga_{0.1}Al_{0.9}As$ window layer on a $pGa_{0.7}Al_{0.3}As$ layer on an $nGa_{0.7}Al_{0.3}As$ layer ($E_g \sim 1.9eV$) on the substrate.

In addition, experimental growths were begun with p^+GaAs single-crystal substrates for preparation of heavily doped $p^+Ga_{0.7}Al_{0.3}As$ layers and then $n^+Ga_{0.7}Al_{0.3}As$ layers, in order to study the electrical properties of the resulting n^+-p^+ interface in GaAlAs, the interface expected to be a low-resistance tunneling junction when properly doped on the two sides. The first experiments gave layers having reasonable surface morphology, but cross-contamination of the melts caused by incomplete wipe-off resulted in compensated and only lightly doped n-type GaAlAs layers, and thus only rectifying junctions were obtained.

Several possible methods for avoiding this difficulty were investigated, including changes in the LPE boat design. A special boat design was developed, and considerable effort was devoted to finding an outside vendor capable of undertaking the difficult fabrication tasks required by the design. A completed prototype was finally received from the selected fabricator in the ninth month of the program, at which time growth experiments were again undertaken in the GaAlAs-GaAs materials system.

Some minor modifications in the boat were found necessary, and when these were completed and the boat satisfactorily cleaned several attempts were made to grow GaAlAs layers of the properties required for use in a GaAlAs (1.7eV)-GaAs two-cell SMBSC connected by a conducting or tunneling junction. Unfortunately, a leak in the H_2 purifier diaphragm occurred at about this time and made the first growth experiments unsuccessful, but the experiments were resumed after repair of the purifier.

The LPE growth procedures with the new boat were improved to allow routine and reproducible growth of the desired layer thicknesses and alloy compositions. Several types of alloy cell structures were fabricated and characterized. The structures grown included those shown schematically in Figure 103.

Complete small-area cells were fabricated and characterized in structures of both the conventional grown-layer type and the Zn-diffused type, as shown at (a) and (b), respectively, in Figure 103. Some of the results are shown in Figures 104, 105, and 106, in which typical illuminated I-V and dark log I-V, sprectral photoresponse, and photoluminescence data, respectively, are given.

In general, these LPE cells were found to have good fill factors (typically 0.7-0.8) but relatively dissappointing V_{oc} and I_{sc} values. On the basis of the deduced Al content, indicated by the bandgap cutoff of the photoresponse curve, the V_{oc} values should be about 100mV higher than those values typically observed. The I_{sc} values should be larger than those measured by a factor of 2 to 5. As is evident in the typical photoresponse curve of Figure 105, there was very poor utilization of the short-wavelength end of the incident illumination by these cells. It appears that increasing the Al content of the window layer and optimizing the thickness of the window layer and the junction layer would improve this considerably.

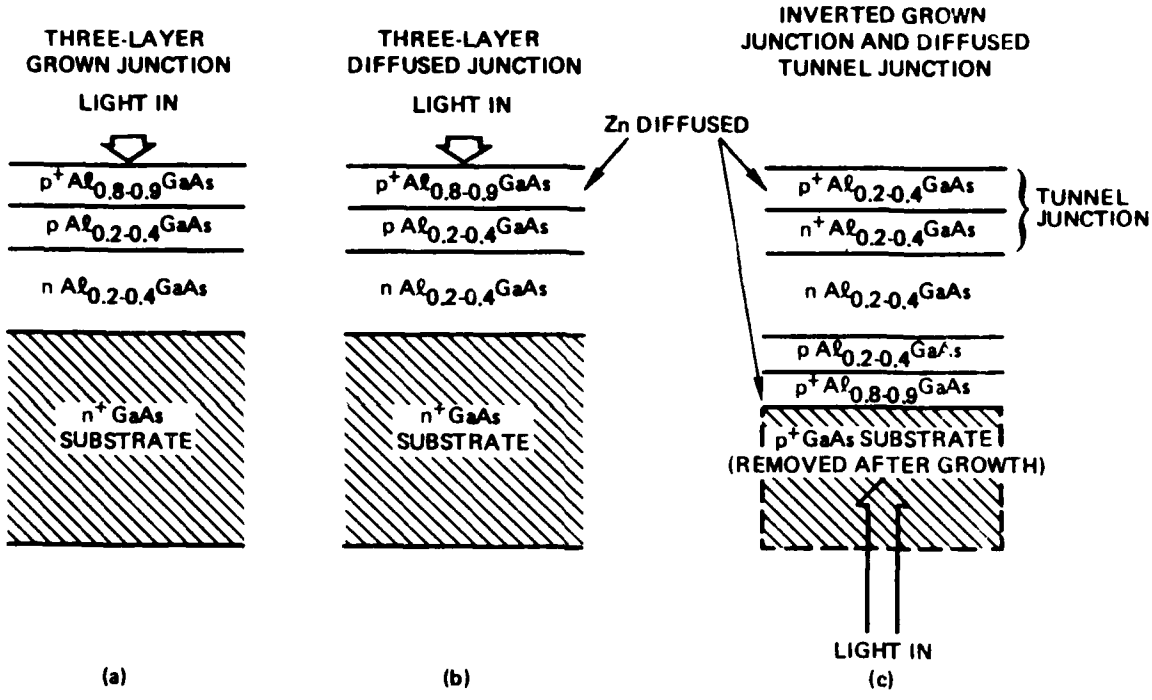


Figure 103. Three GaAℓAs Large-bandgap Solar Cell Structures Grown by LPE Techniques, for Eventual Use in Two-cell and Three-cell SMBSC's

Accordingly, some modifications were made in the parameters of several LPE-grown window-type alloy cell structures that were prepared late in the Phase 1 program. The principal physical parameters of two of those structures are listed in Table 10.

Table 10. Principal Physical Parameters of LPE GaAℓAs Heteroface Solar Cell Structures*

Sample No.	Nominal Aℓ Concentr. (x) in Window	Nominal Window Thickness (μm)	Nominal Aℓ Concentr. (x) in Junction	Nominal Junction Depth (μm)	Type of Junction Processed	Nominal n Layer Thickness (μm)
LPE 1009	0.80	1.43**	0.30	1.0	Zn diffused	7.0†
LPE 1011	0.80	0.57**	0.30	1.0	"	4.7†
"	"	"	"	1.0††	As grown	"

*Structures grown on (100) GaAs substrates at ~800°C.

**Measured in SEM.

†Measured in optical microscope.

††Found to be 0.71μm by measurement.

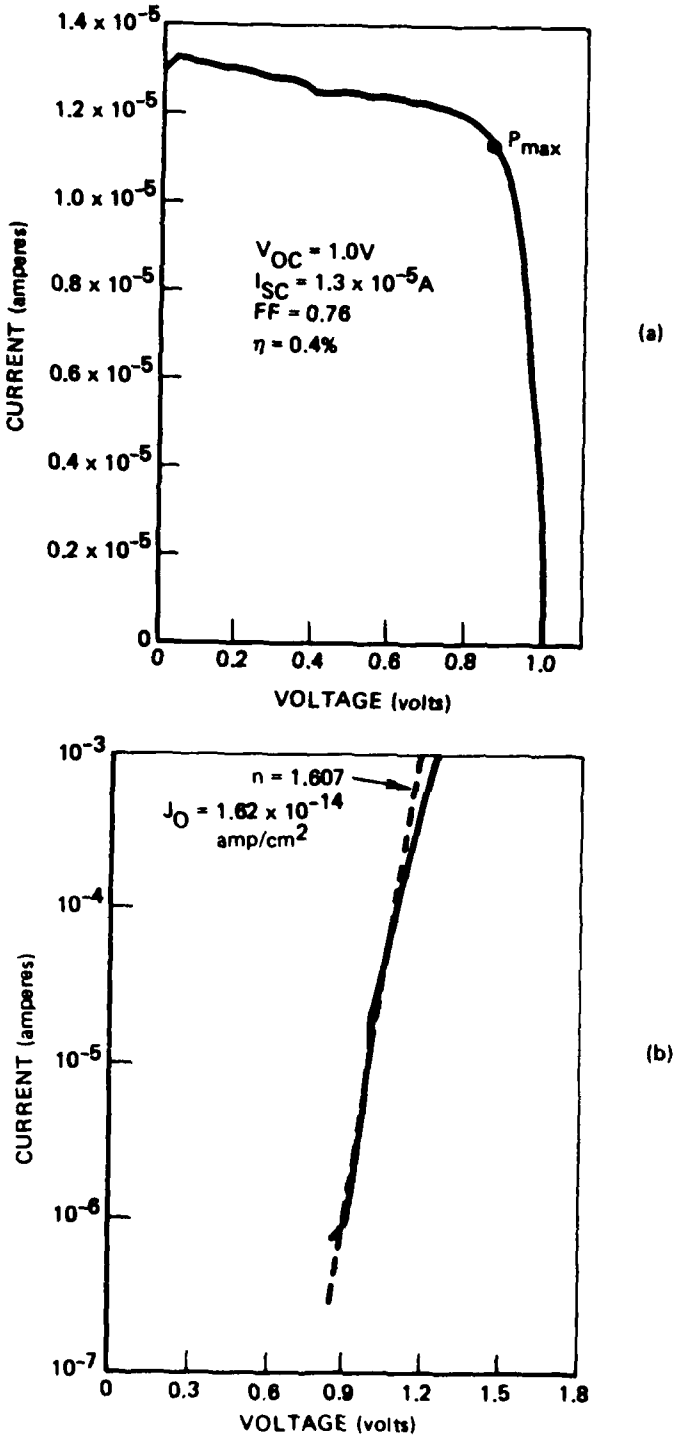


Figure 104. Typical a) Illuminated I-V Characteristic and b) Dark Log I-V Characteristic of Zn-diffused-junction Window-type $Ga_{0.61}Al_{0.39}As$ Solar Cell Grown by LPE (Type b, Figure 103)

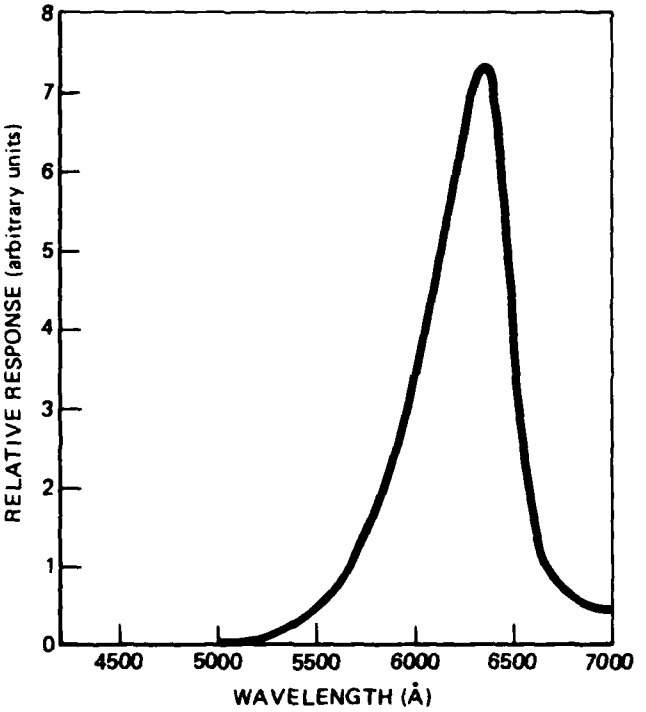


Figure 105. Typical Spectral Photoresponse of Zn-diffused-junction Window-type $Ga_{0.61}Al_{0.39}As$ Solar Cell Grown by LPE (Type b, Figure 103)

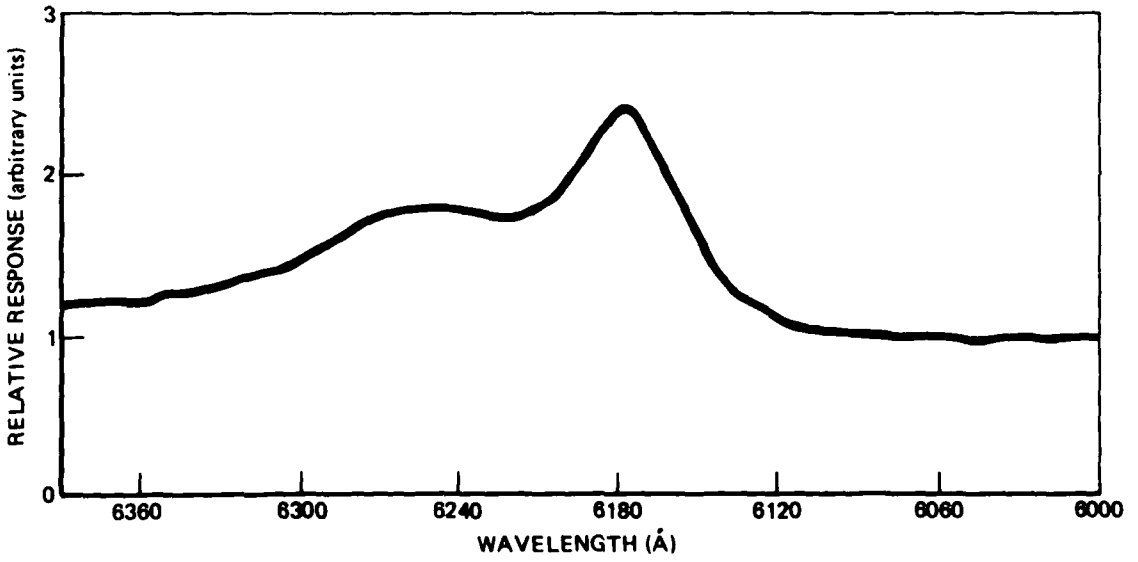


Figure 106. Typical 77°K Photoluminescence Data for Conventional LPE-grown Window-type $Ga_{0.61}Al_{0.39}As$ Solar Cell (Type a, Figure 103)

The first structure (sample LPE1009) was grown with the two-layer configuration $pGa_{0.20}Al_{0.80}As/pGa_{0.61}Al_{0.39}As/n^{+}GaAs$ (substrate), after which Zn was diffused through the upper (window) layer to form the three-layer structure $p^{+}Ga_{0.20}Al_{0.80}As/p^{+}Ga_{0.61}Al_{0.39}As/nGa_{0.61}Al_{0.39}As/n^{+}GaAs$ (substrate). The advantage of this procedure is that only two LPE layers, rather than three, need be grown. The Zn diffusion increases the conductivity of the window layer so that ohmic contact can be easily made, without the necessity of etching through the window layer to make contact directly to the p-type active layer. However, the window thickness (~1.4 μm) on this structure was larger than intended, so it was difficult to control the Zn diffusion depth. As a result, the Zn penetrated too far into the structure in this sample.

The other structure (sample LPE1011, Table 10) was similar dimensionally to those prepared by MO-CVD except for the somewhat thicker (~0.6 μm) window layer. It was grown initially as a three-layer structure, distinguishing it from sample LPE 1009. The junction depth in this sample (p layer thickness, Table 10) must have been close to optimum, judging from the short-circuit current density of 8.5mA/cm^2 obtained with AM0 illumination and no AR coating.

The measured performance parameters for these LPE cells are given in Table 11. The as-grown cell measured on the three-layer sample LPE1011 is seen to exhibit an efficiency of ~4.6 percent and a good fill factor of 0.74. However, the cell processed with Zn diffusion for this structure had a much lower short-circuit current density and a much lower conversion efficiency (although good V_{oc} and fill factor) than did the as-grown cell.

Table 11. Measured Photovoltaic Properties of LPE-grown GaAlAs Heteroface Solar Cells Listed in Table 10 (AM0 simulated illumination).

Sample No.	Type of Junction Processed	Deduced* Al Concentr. (x) in Junction	Nominal Junction Depth (μm)	V_{oc} (volts)	J_{sc} (mA/cm^2)	Fill Factor	Efficiency (%)
LPE1009	Zn diffused	0.39	1.0	1.005	0.51	0.759	0.29
LPE1011	"	0.24	1.0	1.050	2.57	0.767	1.53
"	As grown	"	1.0**	0.970	8.53	0.742	4.55

*Al content of junction layers deduced from long-wavelength cutoff in measured spectral response curve.

**Found to be 0.71μm by measurement.

The spectral response curves for the Zn-diffused cell LPE1009 and the as-grown cell of sample LPE1011 are shown in Figure 107. The as-grown cell of sample LPE1011 shows much better blue response as well as much higher overall response, as indicated also by the J_{sc} values in Table 11. This result is consistent with expectations based on the difference in junction depths in the two structures.

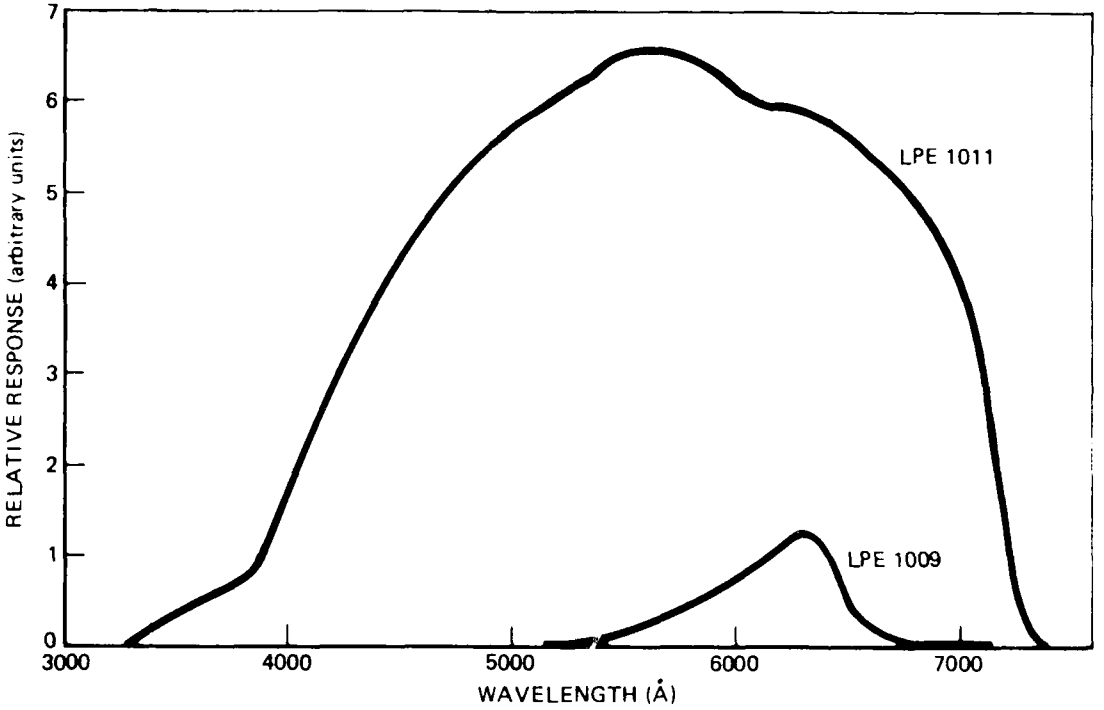


Figure 107. Spectral Response Curves for Zn-diffused Heteroface Cell LPE1009 and As-grown Heteroface Cell of Sample LPE1011 (see Tables 10 and 11)

2.5.2 LPE Growth of InGaAsP

The study of LPE growth of InGaAs layers in Task 3 (Section 2.3) provided a preliminary basis for the growth of InGaAsP layers also by the LPE process.

Early in the program experiments were undertaken to grow InGaAsP by LPE at ERC Thousand Oaks, for possible use as the 1.0eV cell material for a three-cell SMBSC consisting of GaAlAs, GaAs, and InGaAsP cells in series. The specific multilayer structure that was prepared consisted of four epitaxial LPE layers grown on a single-crystal substrate wafer of n^+InP. The layers were, from top to bottom, 1) pInP, 2) pInGaAsP, 3) nInGaAsP, and 4) nInP. Although x-ray analysis of the quaternary layers confirmed a composition of $In_{0.75}Ga_{0.25}As_{0.5}P_{0.5}$, indicating a lattice match to InP and a bandgap energy of ~1eV, measurements of photovoltaic response showed a cutoff at ~0.95 μm, which corresponds to the InP band edge.

It was speculated that Zn diffusion from the p-type layers grown as the final two steps in the LPE growth sequence moved the active p-n junction from the interface between the two quaternary layers to some location within the original n-type buffer layer of InP. Possible solutions to that situation involved reduction of the amount of Zn in the melt and shortening of the duration of growth of the Zn-doped layers (the upper two layers), to attempt to reduce the Zn diffusion that appeared to be occurring near the end of the growth sequence.

However, these possibilities were not pursued further with the InGaAsP materials system. The question of Zn diffusion was addressed in the work with the LPE growth of InGaAs layers in Task 3 (Section 2.3), but all LPE growth studies in this materials system were finally curtailed when the program emphasis was changed later in Phase 1.

2.6 DEVELOPMENT OF AR COATING TECHNOLOGY

This task (Task 7) was intended to include the development of materials and processes to be used for fabricating the required AR coatings for the candidate cell assemblies considered for eventual use in Phase 2 of the program. It was originally planned that such developments would be completed before the end of the first phase of the program, so that the performance of candidate SMBSC's could be established with AR coatings to provide the basis for selection or rejection of each for further development.

The plan originally developed to achieve that goal involved starting the work on the materials and processes for AR coatings for the two-cell SMBSC configurations in the seventh month of the program and continuing it to the end of Phase 1, while that on the coatings for the three-cell composites was to begin in the tenth month and continue through the remainder of Phase 1. In both cases, appropriate materials and the processes for producing them in multilayer coatings that would result in reduction of reflection losses throughout the wide band of wavelengths for which the SMBSC is potentially effective as a power converter were to be identified. This work was to be based in part on the modeling studies of Task 1 and in part on results of experimental measurements of reflection losses in the various multilayer structures grown in Tasks 2-5, inclusive. The modeling studies were expected to identify optimum coating material parameters and number of layers in the AR coatings for various composite cell structures.

Experimental multilayer coatings were also to be prepared in this task. The stability of those experimental coatings under AM0 illumination was to be established, as was the effectiveness of each coating in improving cell performance. Based on such measurements, required changes in material compositions or in multilayer configurations and/or formation techniques would then be made to achieve the necessary AR coating characteristics for the candidate SMBSC configurations.

After the program began it became clear that experimental development of AR coatings should be delayed until other aspects of the experimental program had advanced further. The multilayer AR coating design calculations that were carried out as part of the Task 1 activities (see Section 2.1.1) were a prerequisite to the development of practical AR coatings and coating procedures, but there was no corresponding experimental preparation or development of the specific coatings indicated by those calculations.

Development and application of suitable AR coatings will be involved in the Phase 2 program, as selected SMBSC structures are further developed and require optimized performance conditions.

3. SUMMARY AND CONCLUSIONS

A 14-month (Phase 1) program of experimental investigation backed by analytical modeling has been conducted to develop technologies required for fabricating stacked multiple-bandgap solar cell assemblies having AM0 1-sun efficiencies of 25 percent or greater at 25°C. Investigations were undertaken in the following four SMBSC materials systems, in accordance with the requirements of the contract: 1) two-cell GaAs-Ge structure, made by MO-CVD and conventional CVD methods; 2) two-cell GaAs-InGaAs structure, made by LPE techniques; 3) three-cell GaAlAs-GaAs-GaAsSb structure, made by MO-CVD methods; and 4) three-cell GaAlAs-GaAs-InGaAsP structure, made by LPE methods. After the program began, MBE deposition techniques were added to the investigations of structures 1, 3, and 4. With three months of Phase 1 remaining, a change in program emphasis was introduced by the Air Force to limit the investigations to GaAlAs-GaAs and GaAs-Ge two-cell structures and the three-cell GaAlAs-GaAs-Ge structure that might also result. Principal emphasis was to be on the MO-CVD technique, supplemented by MBE, LPE, or other deposition and/or processing techniques when appropriate for achieving the program goals.

The work carried out during the Phase 1 program is summarized below, by task.

Task 1. SMBSC Modeling and Analysis

Previous work at Rockwell on the modeling of GaAs solar cell performance, both for normal one-sun illumination and for high-concentration (multiple-sun) illumination conditions, was used as the starting point for analytical studies of Ge solar cell performance, GaAlAs heteroface cell performance, spectral photoresponse of thin-window GaAs cells, and multilayer AR coating design.

The Ge cell modeling showed that the cell response for energies below the Ge direct bandgap (i.e., for $\lambda > 1.5\,\mu m$) drops very rapidly, even for a wafer-based $p^{++}/p^{+}/n$ cell structure and a substrate thickness of $300\,\mu m$, due to the limited optical absorption in the indirect-bandgap region ($1.5 \leq \lambda \leq 1.8\,\mu m$). Addition of a back-surface field (BSF) by formation of an $n\text{-}n^{+}$ junction at the rear of the structure has little effect, for the same reason. However, the BSF was shown to be quite advantageous in very thin Ge cells (e.g., all-deposited structures a few μm thick) for energies above the direct bandgap – especially in the region $0.9 \leq \lambda \leq 1.5\,\mu m$.

Modeling the performance of GaAlAs alloy heteroface cells having the structure $p^{+}Ga_{1-y}Al_{y}As/pGa_{1-x}Al_{x}As/nGa_{1-x}Al_{x}As$ ($y = 0.8$-0.9, $x = 0.2$-0.3) and matching the modeled response to the experimentally determined spectral responses of such cells made by the LPE technique allowed estimates to be made of minority carrier diffusion lengths in the junction layers of these devices. This procedure indicated this parameter to be $\sim 0.5\,\mu m$, in substantial agreement with empirically deduced values for the same parameter in the junction layer of similar device structures grown by the MO-CVD process.

Similar matching of modeled and measured spectral photoresponses for thin-window GaAs cells made by the MBE technique was undertaken to obtain estimates of certain cell parameters and to provide some guidance in cell design. However, satisfactory match was not obtained unless window-layer thicknesses much larger than those known to be involved were assumed or much different reflectivity values than those used in the correction of the experimentally determined photoresponse data were introduced. Based on these results it appears that specific reflectivity measurements must be made for each window-type cell evaluated if correct internal photoresponse curves are to be obtained.

Analytical modeling techniques were also employed to develop an algorithm for use in specifying the design parameters of n-layer AR coatings, where $n \geq 3$, for application to SMBSC assemblies; these have spectral ranges broader than those of any of the single cells involved. Some extension of the spectral range covered by two-layer AR coatings was shown to be possible by design changes, but it was found that far better broad-range coverage (e.g., 0.3-1.8 μm for two-cell or four-cell assemblies and 0.3-1.2 μm for three-cell assemblies) can be achieved with three-layer coatings employing MgF_2 or CaF_2 for the top layer, SiO_2 for the middle layer, and Ta_2O_5 or TiO_2 for the bottom layer. Several specific multilayer coatings were designed, although there was no experimental development of these designs in Task 7 because the status of the contract work in Phase 1 did not require it.

Task 2. GaAs-Ge SMBSC Technology Development

Investigation of the two-cell GaAs-Ge SMBSC structure received considerable emphasis. Initially, exclusively the MO-CVD process was used for growth of the GaAs heteroface cells and conventional CVD, utilizing the pyrolysis of GeH_4 in H_2, for deposition of the Ge cell structures. Later in the program, however, the MBE technique was incorporated in the investigations for growth of both GaAs and Ge cells.

Attention was given to two possible SMBSC configurations. The preferred one involved an epitaxial GaAs heteroface cell on an epitaxial conducting junction (either an n^+/p^+ junction in GaAs or an n^+GaAs/p^+Ge heterojunction) on an epitaxial Ge cell, all grown on a single-crystal n^+Ge substrate wafer. The other involved a GaAs heteroface cell epitaxially grown on the front face of a single-crystal n^+GaAs substrate wafer and an inverted n/p Ge cell grown epitaxially on a p^+Ge epitaxial layer deposited on the back face of the n^+GaAs and forming the conducting intercell junction. These configurations required reestablishing or developing satisfactory deposition parameters for achieving high-efficiency GaAs heteroface cells, developing deposition (or other) procedures for preparing good Ge cells, and developing methods for making conducting intercell junction structures. The combining of these components into functioning two-cell stacked assemblies was accomplished late in the program, but performance characteristics were not fully established.

The GaAs heteroface cells prepared on GaAs substrates by the MO-CVD process early in the program were decidedly inferior to those prepared in essentially identical configurations in earlier studies at Rockwell. Contact definition and metallization and series resistance problems were responsible for part of the situation initially. The possibilities of continued processing difficulties and unidentified impurities entering the cell structures from a reactant source tank were examined systematically to attempt to identify the cause, but no single obvious problem was isolated.

Gradual improvement in MO-CVD GaAs cell performance continued throughout the program, however, to the point that cells with $V_{oc} = 0.97V$, $J_{sc} \approx 20mA/cm^2$, fill factor ≈ 0.8 and $\eta = 11.5$ percent (AM0, no AR coating) were being made by the fourth quarter. Use of a good AR coating would increase the AM0 efficiency of such cells to ~16.5 percent which, although not as high as the previous best performance achieved at Rockwell in MO-CVD cells, was quite adequate for the purpose. Further, a very high degree of uniformity of MO-CVD cell performance over the area of substrates up to 2 cm x 4 cm was demonstrated by measurement of I-V characteristics and spectral photoresponse of individual 0.5 cm x 0.5 cm cells processed in arrays on such substrates, illustrating one of the major strengths of the MO-CVD process for large-area cell growth. It did not appear that variation in deposition temperature within the preferred 700-750°C range produced significant differences in overall cell performance, but thinner GaAlAs window layers (500-800Å) and thinner p layers (~0.75 μm) in the active GaAs region did appear to give generally improved photovoltaic response.

GaAs heteroface cells grown by MO-CVD on Ge substrates, however, consistently had higher leakage currents and generally poorer photovoltaic properties than those prepared with nominally the same parameters on GaAs substrates. The best cells on Ge typically had parameters of $V_{oc} = 0.96$-$0.98V$, $J_{sc} = 16$-$17mA/cm^2$, fill factor = 0.70-0.75, and η = 8-9 percent (AM0, no AR coating). Uniformity of cell performance over the area of a large substrate was also not as good as that typically found for cells grown on GaAs substrates, indicating possible non-uninformities in the properties of the Ge substrate material used. Although device processing used early in the program may have been responsible for some of these effects other factors were probably dominant. Lower junction leakage and generally better cell performance were obtained when the Ge substrates were coated with ~1000Å of sputtered SiO_2 (except on the growth surface) to prevent interaction of the substrate and the MO-CVD reactant atmosphere. However, no attempt was made to evaluate the physical integrity of these coatings or to determine an optimum thickness or deposition procedure.

Analysis by Auger electron spectroscopy of the interfacial region of epitaxial GaAs films grown by MO-CVD on (100)-oriented Ge substrates showed the width of the transition region to be dependent upon the specific experimental conditions used during initiation of the GaAs layer growth. A minimum "interface width" of ~45Å resulted when the TMG and the AsH_3 were introduced simultaneously into the deposition chamber to start GaAs growth. This was not the standard procedure, however. Clear evidence was found (primarily by x-ray topographic analysis) that GaAs-Ge structures grown with the standard predeposition procedure, involving exposure of the substrate to AsH_3 for several minutes prior to introduction of the TMG to initiate GaAs growth, have a more defective interface region than do those prepared with a modified procedure in which the exposure to AsH_3 is of only a few seconds duration. However, less conclusive results were obtained for the photovoltaic performance of resulting GaAs cells in the two cases, although the modified procedure does appear preferable, especially in terms of the cell fill factor. Further investigation of this problem is required to provide more conclusive evidence.

Differences among MO-CVD cells on GaAs and on Ge substrates were most distinct in the short-circuit current densities achieved, indicative of low photocurrent

collection efficiencies probably associated with low minority carrier diffusion lengths in the defected GaAs layer adjoining the Ge. Modified cell design (layer dimensions and doping impurity concentrations) and improved substrate quality are expected to result in improved cell performance. No sharply defined preferred temperature was observed for GaAs cell growth on Ge, although the 700-750°C range was again preferred, with generally higher junction leakage currents resulting for higher temperature growth and junction leakage plus excessive series resistance occurring for growth temperatures below ~690°C.

Heteroface GaAs cells formed by the MBE process on GaAs substrates were of generally good quality, even though relatively little program effort was devoted to exploiting the MBE technique for that purpose. The best cell performance was represented by the following parameters: V_{oc} = 0.94V, J_{sc} = 17.2mA/cm^2, fill factor = 0.84, and η = 10.1 percent (AM0, no AR coating); with a good AR coating such a cell would have an AM0 efficiency of over 14 percent. GaAs layers and nGaAs/pGaAs junction structures were grown by MBE on Ge substrates and were of generally high quality, although the junction structures appeared also to involve a pGaAs-nGe heterojunction formed unintentionally at the GaAs-Ge interface. Further investigation of such MBE structures was in progress at the end of the Phase 1 program and is expected to continue into Phase 2.

Formation of Ge solar cells was undertaken by conventional CVD techniques (GeH_4 pyrolysis in H_2) and by MBE methods; limited experiments were also done with spin-on oxide impurity sources to produce junction structures in bulk Ge wafers by thermal diffusion procedures. Since the most attractive configuration for the two-cell GaAs-Ge SMBSC is that in which the Ge cell, the connecting junction, and the GaAs cell are grown in sequence on a single-crystal Ge substrate, most program emphasis was on the formation of Ge cell structures on Ge substrates.

Although the GeH_4 pyrolysis reaction in H_2 can be used in the temperature range ~550-850°C, the best results were obtained at the higher temperatures (~800°C), where the structural quality and surface morphology of the epitaxial films are best and the efficiency of incorporation of dopants (especially B from B_2H_6) is highest. Unfortunately, the stability of the substrate – whether Ge or GaAs – is reduced at those temperatures, and some difficulties with out-diffusion of Sb (or other impurity) from Ge substrates and with As loss at the surface of GaAs substrates (with attendant liberation of Ga metal and subsequent entry into the growing Ge film) were encountered if lengthy deposition experiments were undertaken. The fact that relatively high Ge deposition rates (up to ~0.7 μm/min) could be achieved at the higher temperatures allowed relatively short growth times for most Ge layer thicknesses. However, if prolonged depositions for very thick layers were to be necessary this could become a problem requiring further attention.

The Ge cell performance results improved considerably when the deposition experiments were transferred from a GaAs MO-CVD reactor system to one that had previously been used only for Si CVD. Ge cell structures were then made by growth of B-doped p-type layers on either undoped n-type layers or directly on doped n-type Ge substrate wafers. The best cells had the following characteristics: V_{oc} 190-200mV, J_{sc} = 31-33mA/cm^2, fill factor = 0.65, and η = ~3 percent (AM0, no AR coating); with a good AR coating to reduce reflection losses an AM0 efficiency

of ~4 percent would result for such a cell. It is clear that intentionally doped n-type layers, rather than the nominally undoped n-type layers used in all of the cell structures investigated, must be employed to improve the photovoltaic properties of the CVD Ge cells. Also, relatively minor changes in cell design parameters – especially layer thicknesses and doping concentrations – should result in significant improvements in cell performance. Modifications in the Ge cell contacting procedures (especially the contact alloying schedules) are required to allow maximum device performance to be achieved for any cell design. These improvements should be pursued in the Phase 2 investigations.

Ge cell structures were also made by MBE techniques late in the Phase 1 program. A layer of As of appropriate thickness was deposited on p-type (100) Ge in the MBE apparatus and subsequently diffused at elevated temperature to produce a diffused n-p junction. The resulting cells, although not as good as those formed by CVD, were adequate for use in preparing two-cell stacked GaAs-Ge structures by MBE techniques.

Connecting intercell junction structures for GaAs-Ge SMBSC's were made in GaAs by both MO-CVD and MBE as well as by a combination of the two deposition techniques. Although a few n^+GaAs/p^+Ge heterojunction structures were grown by MO-CVD early in the program, attention shifted at an early date to n^+GaAs/p^+GaAs and p^+GaAs/n^+GaAs structures grown on GaAs and Ge substrates. Deposition temperatures ranged from 630 to 750°C, with generally better results being obtained at the lower temperatures (≤650°C). Good tunnel junction characteristics were obtained in p^+/n^+ structures (each region ~0.6 μm thick) grown at 650°C on GaAs substrates, with peak-to-valley ratios of 4:1 and peak current densities up to ~100 mA/cm^2. Good tunneling characteristics were also obtained in n^+/p^+ structures of similar dimensions grown at ~630°C, with an almost linear I-V characteristic indicating very high conductivity – more than adequate for use as an intercell connection under 1-sun AM0 conditions.

Despite the fact that preliminary annealing tests of some of the tunnel diode structures indicated that the tunneling characteristics might not survive subsequent elevated temperature processing required for growth of the top cell in a stacked cell assembly, the n^+/p^+ GaAs structures grown at 630°C were used in producing the first two-cell GaAℓ As-GaAs SMBSC's. (Similar SMBSC structures employing n^+GaAℓ As/p^+GaAℓ As as the connecting junctions were also prepared, but only the structures with the connecting junction in the GaAs exhibited tunneling properties.) The extent to which the MO-CVD tunnel diode structures, which involve Zn as the p-type dopant and Se as the n-type dopant, would consistently survive subsequent elevated-temperature processing remained an unanswered question to the end of the Phase 1 program and will require further investigation in Phase 2.

However, the formation of p^+GaAs layers by MBE techniques with Be, a slow-diffusing impurity in GaAs, as the added acceptor provided a possible alternative solution to this problem. A hybrid n^+/p^+ tunnel junction structure, consisting of n^+GaAs:Se formed by MO-CVD at ~630°C on p^+GaAs:Be formed by MBE on a GaAs:Cr substrate, exhibited usable tunneling properties, although not as good as those of the all-CVD structure grown at 630°C. Tunnel junction structures of n^+GaAs:Sn/p^{++}GaAs:Be, with thick (~1μm) layers deposited entirely by MBE techniques on p^+GaAs single-crystal substrates at ~540°C, exhibited ohmic behavior.

When thinner (~500Å) junction layers were used similar low-resistance ohmic conduction resulted. Thermal cycling tests of both structures showed that there were no adverse effects on the high conductance of either one following exposure to a temperature-time cycle typical of that involved in LPE growth of a window-type GaAs solar cell structure. It thus appears that a satisfactory connecting junction that will survive subsequent high-temperature processing can be made in GaAs by the MBE technique.

Experimental two-cell GaAs-Ge stacked assemblies were made entirely by MBE techniques and by combined MO-CVD and MBE near the end of the Phase I program, but no such assemblies were completed using CVD techniques exclusively. The all-MBE structure appeared to contain a complicated double heterojunction rather than the intended two-cell and tunnel-junction structure. The hybrid structure involved a heteroface GaAs cell grown by MO-CVD at 750°C on an n^+GaAs:Se/p^+GaAs:Zn tunnel junction grown by MO-CVD at 630°C on a Ge cell structure made by MBE techniques. Processing of this stacked assembly was not completed before the end of Phase 1, however. Additional SMBSC structures involving GaAs and Ge cells prepared by various combinations of CVD and MBE techniques are expected to be prepared and evaluated in Phase 2. In particular, structures involving MBE-grown tunnel junctions should be exploited because of the apparent temperature stability of the Be-doped p-type GaAs prepared by MBE.

Task 3. GaAs-InGaAs SMBSC Technology Development

Investigations of the two-cell GaAs-InGaAs SMBSC system to be made by LPE growth methods on n^+GaAs substrates involved principally the experimental growth of InP and InGaAs layers on InP and GaAs single-crystal substrates and an evaluation of the AlGaAsSb materials system as an alternative to InGaAs for the low-bandgap cell of this SMBSC structure.

Experimental LPE growth of p^+InP layers (to serve as the lattice-matched window material for the low-bandgap InGaAs cell) on n^+GaAs substrates was only partially successful. Growth from both In and Sn solvents was studied, with the former producing acceptable growth on (111B)GaAs in a narrow temperature range around 520°C and the latter resulting in rough but marginally acceptable layers on (100)GaAs at higher temperatures (600-800°C) provided that large vertical temperature gradients were maintained across the liquid-solid interface to maintain the substrates below the temperatures normally induced by the process, thus minimizing etch-back. However, high densities of In inclusions persisted at the growth interface, rendering the structures impractical for use in stacked cell configurations. Therefore, to circumvent such difficulties, InP layers were grown separately on GaAs substrates by the MO-CVD process for use in the subsequent LPE growth experiments with InGaAs.

LPE growth experiments were undertaken with the lattice-matched (to InP) ternary composition $In_{0.52}Ga_{0.48}As$. Several p-n junction structures were grown, initially on single-crystal (111B) InP substrates. Despite some problems in making ohmic contacts, these structures were characterized and found to have low current collection efficiency as well as questionable stability of location of the junction, due to probable movement of Zn (the p-type dopant) during the LPE growth process.

There was also some evidence that an InP-InGaAs heterojunction had resulted, producing defect-assisted tunneling currents rather than simple p-n junction characteristics.

Growth of thicker undoped InGaAs layers at relatively low temperatures (~630°C) on polished (111B)-oriented p⁺ InP substrates, with slight substrate etch-back prior to growth, resulted in n-type material of approximate composition $In_{0.53}Ga_{0.47}As$ (bandgap energy ~0.7 eV) in which a junction was evidently formed by Zn out-diffusion from the substrate. Solar cells fabricated from this material exhibited V_{oc} values < 0.1V and J_{sc} values of ~16mA/cm^2 (AM1, no AR coating), with the low photovoltages attributed to large J_o values and poor diode factors. There was some indication that an additional barrier – perhaps a heterojunction at the InGaAs-InP interface – had been formed during the growth process.

Some preliminary experiments were then undertaken with growth of InGaAs on the MO-CVD InP/GaAs composite samples previously prepared, but discontinuous layers with poor melt wipeoff were obtained, probably due to the extreme caution exercised in attempting to avoid loss of the relatively thin InP layers by meltback as growth was being initiated. The work was not pursued further, however, because of the change in technical emphasis introduced late in the program.

When the problems were first encountered in the InP/InGaAs system early in the program some attention was diverted to AlGaAsSb as a possible alternative small-bandgap cell material. Window-type cell structures were grown on n-type single-crystal GaSb substrates by LPE with the configuration $pGa_{0.7}Al_{0.3}AsSb/pGaSb(undoped)/nGaSb(substrate)$, but poor photovoltaic properties (especially fill factor and short-wavelength response) were obtained. Modified structures, with improved contacts to reduce series resistance and thinner pGaSb layers to improve short-wavelength response, were then prepared with the configuration $p^+Ga_{0.7}Al_{0.3}AsSb/pGa_{0.9}Al_{0.1}Sb/nGaSb$ (substrate). Addition of Al to the GaSb p layer reduced the layer growth rate, so that shorter deposition times (~1 min at ~520°C) allowed growth of p layers that were 2-3 μm thick.

These changes allowed attainment of cells with the parameters V_{oc} = 0.240V, J_{sc} = 29mA/cm^2, fill factor = 0.51, and $\eta \approx 3.5$ percent (AM1, no AR coating). Junction leakage and series resistance remained as problems, but the results were sufficiently encouraging to prompt a brief investigation of various contact materials for both p-type and n-type GaSb to attempt to reduce series resistances losses. Pure Au contacts were found best for both conductivity types. Several additional cell structures, including some with higher Al composition (~0.7) in the window layer, were subsequently prepared, but the investigations were not carried further because of the change in program emphasis invoked at that time.

Task 4. GaAlAs-GaAs-GaAsSb SMBSC Technology Development

Investigations of the several technologies required for the three-cell GaAlAs-GaAs-GaAsSb tandem structure were given major emphasis. It was originally expected that exclusively MO-CVD techniques would be used to make this structure, but MBE methods were introduced to supplement the MO-CVD process part way through the program. Also, near the end of Phase 1 the program emphasis was shifted to the GaAlAs-GaAs-Ge materials combination, at which time no further effort was directed to GaAsSb as the small-bandgap material.

The technologies requiring most of the development attention were the growth and fabrication of satisfactory GaAlAs cells with 1.8-2.0 eV bandgaps, the preparation of high-conductance connecting junctions in GaAlAs and/or in GaAs (the latter already described), the growth and fabrication of $GaAs_{0.5}Sb_{0.5}$ 1.0 eV cells by MO-CVD, and the combining of the components into a stacked cell assembly. Experimental studies were conducted in all of these areas except the preparation of GaAsSb cells by MO-CVD; this materials system was investigated briefly using LPE techniques, as noted above, but MO-CVD studies had not been undertaken prior to the time at which the program emphasis was changed.

The experiments with GaAlAs large-bandgap cell structures were essentially all done with n^+GaAs:Si or GaAs:Te substrates. Cell configurations were typically $p\ Ga_{1-y}Al_yAs/pGa_{1-x}Al_xAs/nGa_{1-x}Al_xAs$ ($y \geq 0.8$, $x = 0.2$-0.4), in some cases with a thin p^+GaAs:Zn cap layer on top of the window layer to facilitate contacting the junction layer of the cell. Deposition temperatures ranged from 700 to 800°C, with 750°C the most commonly used. Most completed cells were 0.5 cm x 0.5 cm, although small individual mesa cells in several sizes were also fabricated at times. Good I-V characteristics (dark and illuminated) were obtained with these devices almost from the start. Cell response appeared to improve generally with increasing deposition temperature, and compositions with $x = 0.24$ in the active regions gave better performance than those with $x = 0.3$ or 0.4 in these early devices.

It became clear, from analysis of the performance of the first two-cell GaAlAs-GaAs SMBSC's, that the alloy cells were probably the main limiting factor in performance of the stacked structures. Spectral response measurements on separate alloy cells with various layer dimensions and design parameters showed that reduced short-wavelength responses were responsible for the relatively small J_{sc} values typically obtained with these cells, although the degree of uniformity of response among an array of 15-20 cells formed on a single large GaAs substrate was extremely high. It appeared that poor current collection efficiency (i.e., small minority-carrier diffusion length) in the pGaAlAs active layers was most likely responsible for the reduced high-energy responses. The best parameters observed with alloy cells grown at ~750°C on an n^+GaAs substrate and having the nominal configuration $pGa_{0.2}Al_{0.8}As(1000Å)/pGa_{0.76}Al_{0.24}As(0.6\ \mu m)/nGa_{0.76}Al_{0.24}As(2.4\ \mu m)$ were $V_{oc} = 0.96V$, $J_{sc} = 12.0 mA/cm^2$, fill factor = 0.63, and $\eta = 5.4$ percent (AM0, no AR coating).

Late in the program several groups of alloy cells with window-layer thicknesses from 0.08 to 0.15 μm, and Zn-doped p-layer Al compositions of $x = 0.18$-0.35 and thicknesses ranging from 0.3 to 1.5 μm were grown at ~750°C. It was found that V_{oc} increased as the Al content of the junction-forming layers increased, especially for $x > 0.2$, but the V_{oc} values were appreciably less than the theoretically expected values for all but very low ($x < 0.10$) Al compositions. The highest V_{oc} value observed was ~1.1V for cells in which $x \approx 0.35$. The J_{sc} values were shown to depend upon both Al content and thickness of the window layer as well as the junction layer. Active layer compositions with $x \approx 0.3$ seemed superior, and junction depths less than ~0.7 μm were clearly preferred, with thicker p layers causing reductions in J_{sc}. This indicated that minority-carrier diffusion lengths were probably $< 0.5\ \mu m$ in the GaAlAs p layers made by MO-CVD. Spectral response measurements showed that window layer compositions with $y = 0.9$ allowed better blue response and higher J_{sc} values than those with $y = 0.8$, and window layer thicknesses <800Å were preferred. Most cells had J_{sc} values less than $6 mA/cm^2$ for AM0 illumination, no

matter what compositions or dimensions were involved; fill factors ranged from 0.60 to 0.76 and efficiencies were ≤4 percent (no AR coating).

A few alloy cells were processed with Zn diffused into the window layer to increase its conductivity and produce a front-surface field as a possible means of improving cell performance. Although this procedure did appear to increase the J_{SC} values for some MO-CVD cells, it had the opposite effect for other MO-CVD cells and for the LPE GaAlAs cells on which it was used, so it was not further pursued. As of the end of the Phase 1 program the performance of the GaAlAs cells still required considerable improvement, so continued emphasis in this area is anticipated in Phase 2.

Several attempts were made to achieve tunneling properties in GaAlAs junction structures grown by MO-CVD, beginning early in the program, for the purpose of providing the connecting junction between GaAlAs cells and GaAs cells in stacked assemblies. Both n^+/p^+ and p^+/n^+ junction structures with $Ga_{1-y}Al_yAs$ compositions of y 0.08 to y 0.37 were grown at temperatures of 700 and 750°C, but at best only weak tunneling was observed. Although the emphasis in the remainder of Phase 1 was on tunnel junction structures in GaAs, it is expected that further effort will be devoted to achieving tunneling structures in the alloy in the Phase 2 program since that configuration is preferred in terms of overall performance of the stacked assemblies.

Two-cell GaAlAs-GaAs SMBSC's were fabricated and tested approximately midway through the program, as soon as evidence of tunneling in n^+/p^+ structures in GaAs had been observed. Although such structures were made with the connecting n^+/p^+ junction structure both in GaAs and in GaAlAs, only the former exhibited adequate tunneling properties. The successful configuration was GaAlAs cell/GaAs n^+-p^+ junction/GaAs cell, grown by MO-CVD on an nGaAs:Si substrate. Best results were obtained with a structure in which the alloy cell configuration was
$p^+Ga_{0.2}Al_{0.8}As$:Zn(1000Å)/$pGa_{0.7}Al_{0.3}As$:Zn(0.75 μm)/$nGa_{0.7}Al_{0.3}As$:Se(2.5 μm). The tunneling junction was n^+GaAs:Se(0.4 μm)/p^+GaAs:Zn(0.4 μm) and the GaAs cell was $pGa_{0.7}Al_{0.3}As$:Zn(0.5 μm)/pGaAs:Zn(1.0 μm)/nGaAs:Se(4.0 μm). Growth temperatures were 750, 630, and 700°C, respectively, for the three component regions.

Under tungsten lamp illumination this SMBSC exhibited a V_{OC} of ~2.1V and a J_{SC} of ~4.5mA/cm^2. This represents the first successful achievement of a stacked cell grown completely by a vapor-phase process and exhibiting voltage addition. The V_{OC} value is believed to be the highest achieved up to that time for a stacked cell grown by any process. It appeared that the $Ga_{0.7}Al_{0.3}As$ cell in this structure was probably the limiting component in the performance of the stacked assembly, preventing higher photocurrents from being collected.

Because of some evidence that better alloy cell performance was obtained for higher growth temperatures, some GaAlAs-GaAs stacked structures were grown in which the alloy cell was deposited at 775 and 800°C, but increased leakage currents and lower V_{OC} values were obtained in each case. Further investigation is required to determine if these effects may have been caused by dopant diffusion in the lower layers of the structure during growth of the alloy cell at the higher temperatures. At the end of Phase 1 several additional two-cell stacked structures were grown with

greatly reduced thicknesses in the tunnel junction layers (~100Å each) and the alloy cell deposited at 750°C to attempt to improve the properties of the resulting SMBSC. Initial evaluation of some of the cells, although not complete, indicated that the intended improvements had not been achieved. Thus, work with the GaAlAs-GaAs two-cell tandem structure must be continued into the Phase 2 program in order to realize the overall performance expected of this materials combination.

Task 5. GaAlAs-GaAs-InGaAsP SMBSC Technology Development

The study of the three-cell GaAlAs-GaAs-InGaAsP SMBSC assembly to be made by LPE methods using both surfaces of n⁺GaAs single-crystal substrates involved two main areas of investigation – LPE growth of 2.0 eV GaAlAs cell structures on GaAs surfaces and LPE growth of 1.0 eV InGaAsP layers. Existing well-established methods for LPE growth of GaAs cells provided the third major cell technology. The GaAs (or GaAlAs) tunnel junctions and InP/GaAs tunneling heterojunctions developed in other tasks and employing either LPE or MBE techniques were expected to provide the needed cell interconnections.

Window-type alloy cell structures were grown by LPE on n⁺GaAs substrates early in the program, with the configuration $p^+Ga_{0.1}Al_{0.9}As/pGa_{0.7}Al_{0.3}As/nGa_{0.7}Al_{0.3}As$. Some experimental n^+/p^+ alloy structures were also grown, but incomplete wipeoff in the LPE boat resulted in cross-contamination of the melts and unsatisfactory structures. A special LPE boat was then designed, and fabrication was completed by an outside vendor several months later. Modified LPE growth procedures were developed for use with the new boat, and several types of alloy cell structures were prepared.

Complete small-area window-type cells were fabricated both by conventional processing and by processing that involved Zn diffusion into the window layer. Window-layer Al contents were in the range y = 0.8-0.9 and junction layer Al contents x = 0.2-0.4. The cells generally had good fill factors (typically 0.7-0.8) but relatively low V_{oc} and J_{sc} values. Spectral response curves showed poor utilization of the short-wavelength illumination, indicating needed changes in window layer thickness and junction layer thickness and Al content.

Some additional alloy cells were prepared near the end of Phase 1, including several in which only a p-type active layer and a p-type window layer were deposited in succession by LPE on an n⁺GaAs substrate, followed by Zn diffusion through the window layer and the p layer to produce the active p-n junction, just inside the substrate. However, in the abbreviated investigation it was found difficult to control the diffused junction depth. The cells grown and processed by conventional procedures were somewhat better; J_{sc} values up to 8.5mA/cm^2 and efficiencies up to 4.6 percent (AM0, no AR coating) were obtained. Open-circuit voltages (~1.0V)and fill factors (~0.75) were about the same for both types of cell.

Only limited investigation of the LPE growth of InGaAsP for the 1.0 eV bandgap cell was undertaken. Multilayer structures of the configuration pInP/pInGaAsP/nInGaAsP/nInP were grown on n^+InP substrates. Analysis showed the quaternary layers had the composition $In_{0.75}Ga_{0.25}As_{0.5}P_{0.5}$, indicating a bandgap of ~1eV and a lattice match to InP, but photoresponse measurements showed

cutoff at the InP band edge. This was believed caused by Zn dopant diffusion from the two upper layers into the nInP buffer layer, shifting the active junction to that location. Although the problems of Zn diffusion in LPE growth in the InGaAs system were examined in the Task 3 studies, the investigation of the quaternary was not carried further in Phase 1.

Task 6. Characterization of Materials and Photovoltaic Devices

Descriptions of the activities of this task are included in the other task discussions.

Task 7. Development of AR Coating Technology

There was no experimental development of specific AR coatings for the various SMBSC's investigated during Phase 1. Although multilayer AR coating designs were developed in the Task 1 modeling and analysis studies, the preparation of appropriate coatings was postponed until Phase 2 of the program.

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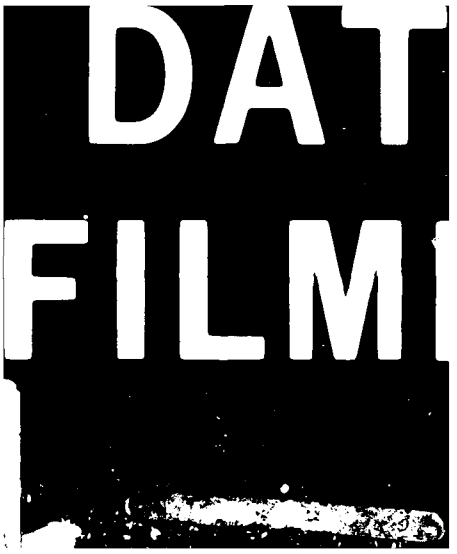
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